FACULTY OF INFORMATION TECHNOLOGY AND ELECTRICAL ENGINEERING
DEGREE PROGRAMME IN WIRELESS COMMUNICATIONS ENGINEERING

MASTER'S THESIS

Voltage Controlled Oscillator for mm-wave Radio Systems

Author	Yasir Shafiullah
Supervisor	Aarno Pärssinen
Second Examiner	Olli Kursu
Technical Advisor	Rehman Akbar

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ABSTRACT

The advancement in silicon technology has accelerated the development of integrated millimeter-wave transceiver systems operating up to 100 GHz with sophisticated functionality at a reduced consumer cost. Due to the progress in the field of signal processing, frequency modulated continuous wave (FMCW) radar has become common in recent years. A high-performance local oscillator (LO) is required to generate reference signals utilized in these millimeter-wave radar transceivers. To accomplish this, novel design techniques in fundamental voltage controlled oscillators (VCO) are necessary to achieve low phase noise, wide frequency tuning range, and good power efficiency. Although integrated VCOs have been studied for decades, as we move higher in the radio frequency spectrum, there are new trade-offs in the performance parameters that require further characterization.

The work described in this thesis aims to design a fully integrated fundamental VCO targeting to 150 GHz, i.e., D-Band. The purpose is to observe and analyze the design limitations at these high frequencies and their corresponding trade-offs during the design procedure. The topology selected for this study is the cross-coupled LC tank VCO. For the study, two design topologies were considered: a conventional cross-coupled LC tank VCO and an inductive divider cross-coupled LC tank VCO. The conventional LC tank VCO yields better performance in terms of phase noise and tuning range. It is observed that the VCO is highly sensitive to parasitic contributions by the transistors, and the layout interconnects, thus limiting the targeted frequency range. The dimensions of the LC tank and the transistors are selected carefully. Moreover, the VCO performance is limited by the low Q factor of the LC tank governed by the varactor that is degrading the phase noise performance and the tuning range, respectively. The output buffer loaded capacitance and the core power consumption of the VCO are optimized. The layout is drawn carefully with strategies to minimize the parasitic effects. Considering all the design challenges, a 126 GHz VCO with a tuning range of 3.9% is designed. It achieves FOM_T (Figure-of-merit) of -172 dBc/Hz, and phase noise of -99.14 dBc/Hz at 10 MHz offset, Core power consumption is 8.9 mW from a 1.2 V supply. Just falling short of the targeted frequency, the design is suitable for FMCW radar applications for future technologies. The design was done using Silicon-on-Insulator (SOI) CMOS technology.

Keywords: Voltage-controlled oscillator, Millimeter-wave, LC, Phase noise, FMCW, CMOS, VCO, Integrated circuits, D-band, Varactor, Quality factor, CMOS SOI, Radar.

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FOREWORD

This Thesis was conducted at the Center for Wireless Communications for Radio Technologies (CWC-RT) research unit at the University of Oulu, Finland. The purpose of this thesis was to design and implement a Voltage Controlled Oscillator (VCO) for FMCW Radar applications targeting an operating frequency of 150 GHz.

I would like to take this opportunity to thank a number of people for their invaluable assistance during the duration of my thesis. I am deeply grateful to my supervisor, Professor Aarno Pärssinen, for his support, patience, motivation, and immense knowledge throughout my thesis. Also, I would like to thank my examiner, D.Sc. Olli Kursu, for his critique and suggestions. I would like to express my heartfelt gratitude to my technical advisor, Rehman Akbar, for his unconditional support, guidance, knowledge, and advice during my thesis. I am grateful to Mikko Hietanen for his technical opinions and views. Many thanks to my colleagues and friends for the needed motivation throughout this work

Lastly, special thanks to my parents for their love, sacrifices, continued moral support, and encouragement during my hardships in life.

Oulu, June 01, 2020

Yasir Shafiullah

LIST OF ABBREVIATIONS AND SYMBOLS

AC	alternating current
DC	direct current
VCO	voltage controlled oscillator
CMOS	complementary metal-oxide semiconductor
BiCMOS	bipolar complementary metal-oxide semiconductor
NMOS	N-type metal-oxide-semiconductor
IC	integrated circuits
LC	inductive-capacitive
Hz	hertz
MHz	megahertz
GHz	gigahertz
THz	terahertz
PLL	phase-locked loop
FMCW	frequency-modulated continuous-wave
SOI	silicon-on-insulator
SCPW	slow-wave coplanar waveguide
Q	quality factor
LO	local oscillator
IF	intermediate frequency
ADC	analog-to-digital converter
DSP	digital signal processing
PVT	process-voltage-temperature
SSB	single-sideband
CCP	cross-coupled pair
FDSOI	fully depleted silicon-on-insulator
mm-wave	millimeter wave
MOS	metal-oxide semiconductor
PA	power amplifier
LNA	low noise amplifier
LPF	low pass filter
PD	phase detector
FOM	figure of merit
FOM_T	figure of merit including tuning range
PN	phase noise
CS	common source
MAG	maximum available gain
SLVT	super low threshold voltage
SRF	self-resonance frequency
RLGC	resistance, inductance, conductance, capacitance
EM	electromagnetic
GND	ground
MOM	metal-oxide-metal
PSS	periodic steady state
G_m	transconductance of the cross-coupled pair
g_m	transconductance of the single transistor in cross-coupled pair

K_{VCO}	voltage controlled oscillator tuning sensitivity
nm	nanometer
μm	micrometer
fF	femtofarad
pH	picohenry
mW	milliwatt
dBc	power ratio of carrier to signal expressed in decibels
t	time
T	time period
Φ_T	phase at time period T
ω	angular frequency
$H(j\omega)$	frequency response
f_{VCO}	VCO oscillation frequency
f_{center}	center frequency
K_{VCO}	VCO gain
V_{TUNE}	VCO tuning voltage
TR	frequency tuning range
f_{max}	maximum frequency
f_{min}	minimum frequency
Δf	difference between the maximum and the minimum frequency
C_{fix}	fixed capacitance
C_{vmax}	maximum varactor capacitance
C_{vmin}	minimum varactor capacitance
Δf_{off}	phase noise at a frequency offset
T_c	time period at the center frequency
f_c	center frequency
$L(\Delta\omega)$	noise spectral density
K	boltzmann's constant
P_{sig}	signal power
ω_o	oscillation frequency
F	noise figure
φ_n	the phase of the signal
a_n	amplitude
C_{var}	varactor capacitance
C_{par}	parasitic capacitance
C_{par_buffer}	buffer parasitic capacitance
$R_{p_{var}}$	varactor parallel resistance
$R_{p_{ind}}$	inductor parallel resistance
F_{osc}	oscillation frequency
X_L	inductive reactance
X_c	capacitive reactance
Q_{ind}	inductor quality factor
Q_{var}	varactor quality factor
Q_{tank}	LC tank quality factor
C_{ox}	oxide capacitance
C_{GD}	gate to drain capacitance
C_{DS}	drain to source capacitance
C_{GS}	gate to source capacitance

TL	transmission line
C_n	neutralization capacitance
K	rollet stability factor
G_{max}	maximum gain
R_{neg}	negative resistance
R_p	parallel equivalent resistance
R_s	series equivalent resistance
F_T	transition frequency
F_{max}	maximum oscillation frequency

1 INTRODUCTION

1.1 Motivation

The advancement in the state of the art technologies, i.e., Complementary Metal Oxide Semiconductor (CMOS) and Bipolar CMOS (BiCMOS) and have paved the way for commercial applications at mm-wave frequencies targeting above 100 GHz at low cost. The large bandwidth and small antennas have made these frequencies attractive for ultra-compact radar systems. Previous work has been done on integrated Frequency Modulated Continuous Wave (FMCW) radar transceiver in CMOS and BiCMOS processes demonstrated at 120-160 GHz [1] [2] [3] [4]. In these transceivers, the Voltage Controlled Oscillator (VCO) plays a vital role in determining the overall performance with respect to phase noise, tuning range, linearity, and output power level. Silicon-on-insulator (SOI) technologies below 40nm have the potential to reach 100 GHz and beyond. The 60 GHz VCO utilizing the back gate control to obtain a wide tuning range of 34% [5] and the low power VCO design at 80 GHz employing Slow-wave Coplanar Wave (SCPW) transmission line instead of on-chip inductor showed promising results to explore and go beyond 100 GHz targeting at 150 GHz [6].

In the past, a few D-Band VCOs have been reported implementing different topologies. A 114 GHz VCO in 0.13 µm CMOS technology with a 2.1% tuning range [7] and 131 GHz VCO in 90 nm CMOS technology with a 1.7% tuning range by P.-C. Huang utilizes push-push topology [8]. A cross-coupled pair enhancement technique in LC based topology was used by Patrick Reynaert at 118 GHz VCO resulting in a 7.8% tuning range with the highest reported figure of merit (FOM_T) of -175.7 dB in 65nm CMOS technology [9]. The Colpitts VCO topology was implemented at 115 GHz and 165 GHz with optimization in phase noise performance [10]. A varactorless topology was presented in [11], obtaining the tuning range by the variation of the supply voltage. As of initial observation, the majority of work at the frequencies above 100 GHz has been done utilizing the push-push and the Colpitts topology. Also, it is noteworthy that in the race to excel at higher frequencies, the 22nm CMOS fully depleted SOI (FDSOI) was not observed to stand out in implementation, which can be seen from Figure 1. This thesis work will look into the potential and performance of the 22nm CMOS process at higher frequencies, i.e., above 100 GHz.

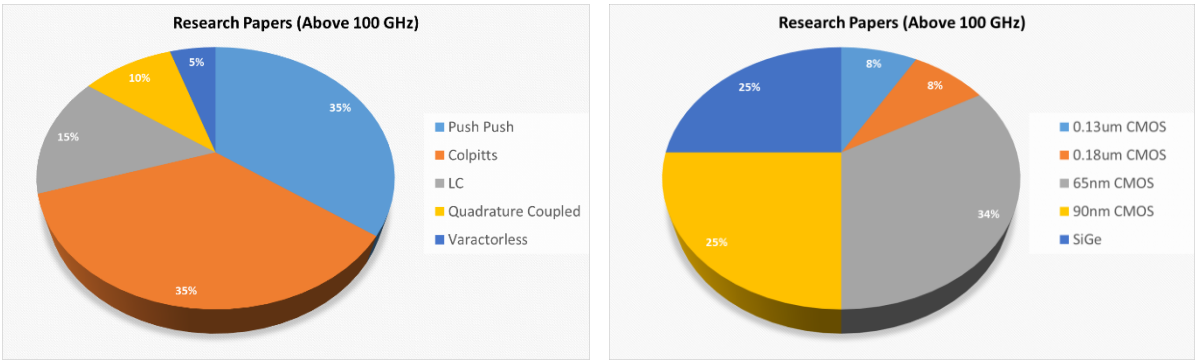


Figure 1. Research paper overview above 100 GHz

At these high frequencies, the major difficulties in the VCO design are low phase noise, wide tuning range, and low power consumption. The overall performance of the VCO is highly dependent on the LC-tank quality factor. As per the Leeson formula [12], the Q factor is inversely proportional to the phase noise. The cross-coupled pair (CCP) will assist in compensating for the losses in the tank. The low Q factor of the tank will ultimately require a

high G_m that requires a large transistor and it will consume more power. At mm-wave, varactors have a low quality factor. For instance, to achieve low phase noise, the varactor shall be chosen of minimum length, and this will eventually reduce the tuning range. Therefore, there is a trade-off between the quality factor, phase noise, power consumption and the tuning range. The motivation of this thesis is to find a proper balance at these high frequencies which is of significance.

1.2 Objective

The objective of this thesis is to design a fully integrated VCO in 22 nm FDSOI CMOS with a wide tuning range and low phase noise targeting to 150 GHz by utilizing the LC cross-coupled VCO as topology. An LC tank is made by using a single turn center-tapped inductor and an accumulation MOS varactor. The NMOS cross-coupled core is used to produce negative G_m for oscillation. The VCO prototype is implemented to demonstrate the feasibility of LC VCO at high frequencies.

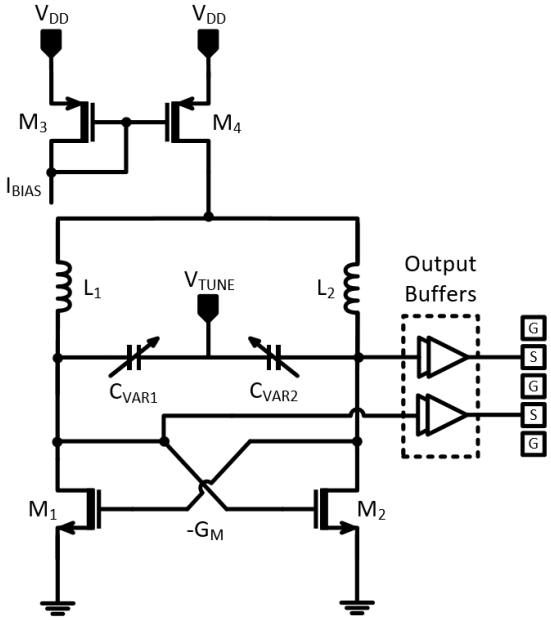


Figure 2. Cross-Coupled VCO Schematic

1.3 Thesis Organization

The thesis aims to explore the performance and limits of the 22nm FDSOI CMOS in a VCO design targeting at an operating frequency of 150 GHz. The thesis is organized as follows:

Chapter 2 presents an introduction to the VCO and the theory of oscillations. A brief look into the design methodologies and the theory behind the LC VCOs will be given. Furthermore, background research with different topologies in practice is discussed.

Chapter 3 illustrates a detailed look into the VCO design and implementation of the circuit, including characterization, simulation and layout considerations. It also discusses the challenges encountered during the design and how they are tackled to obtain the simulation results.

Chapter 4 presents the performance evaluation alongside results obtained from the Final EM simulation with state of the art VCO's.

Conclusion, Discussion, and future work will be summarized in **Chapters 5 and 6.**

2 BACKGROUND INFORMATION

This section focuses on a general overview of the oscillator and design concepts. To begin with, the applications of VCO in FMCW architecture are observed and the basic oscillator theory and its conditions are discussed. The voltage-controlled oscillation theory and its configurations are briefly reviewed. Finally, a cross-coupled LC oscillator is presented with the essential design steps and components that are required to be used in the VCO design.

2.1 VCO and FMCW Radar Applications at Sub-THz

Earlier, discrete components, i.e., power amplifiers (PAs), VCOs, low noise amplifiers (LNAs), and analog to digital converters (ADCs), were utilized in Radar applications. Since integrated solutions are readily available, a single-chip CMOS based radar that integrates all RF, analog and digital signal processing (DSP) capability represent an ultimate solution to system-on-chip radar. The D-band (110-179 GHz) frequency range offers opportunities of silicon technology in short-range radar, passive remote sensing, non-destructive testing with active imaging [13], and high data point to point links [14].

FMCW radar systems have been common in the automotive industry. It is a type of radar system which employs the usage of stable frequency wave radio energy that being transmitted and received from the reflecting objects. The received signal arrives at a different frequency than the transmission, allowing the object to be detected utilizing the Doppler effect. The FMCW radar is implemented in such a way that it contains a VCO which is the local oscillator (LO) module that generates the linear frequency modulated continuous waveform represented by $\cos(\Phi_T(t))$, which is then amplified by the power amplifier and is then transmitted from the antenna. An object present in the line of sight is illuminated by the radar and the transmitted signal is reflected back. The LNA amplifies the reflected signal. It is mixed with LO to generate an intermediate frequency (IF) output, which the ADC digitizes and the DSP processes afterward. In FMCW radar, the transmitted signal is a linear frequency modulated continuous wave (L-FMCW) chirp signal, which is a saw-tooth waveform and its frequency changes linearly with time.

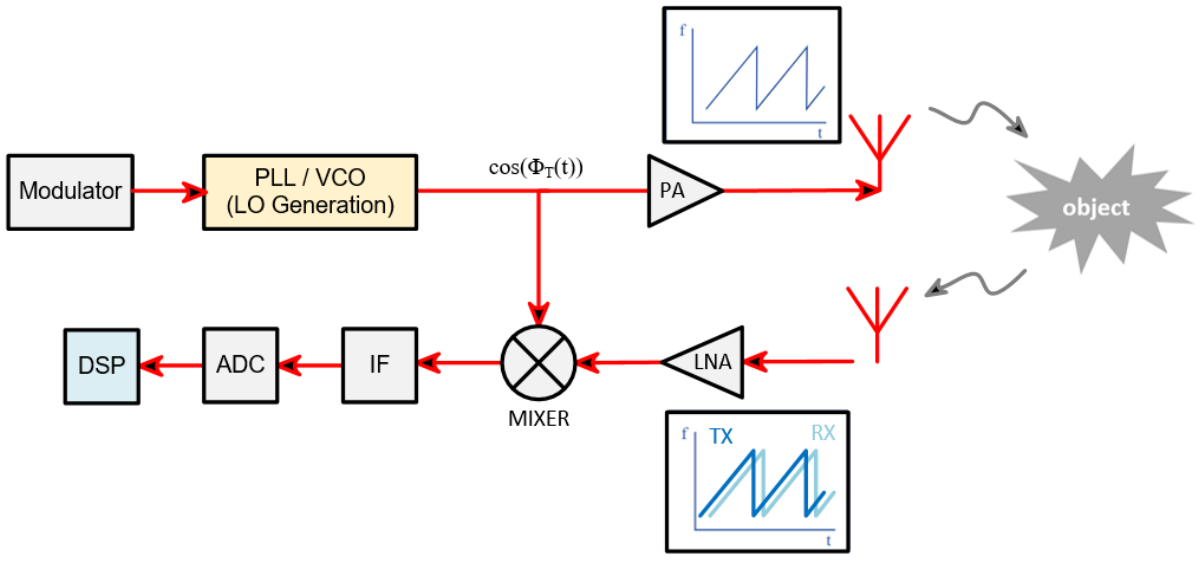


Figure 3. Block diagram of an FMCW Radar

For the efficient application of radar in D-Band, an FMCW synthesizer with high performance, low phase noise, and wideband VCOs is essential. The key parameter that determines the loop performance and phase noise of the PLL is the gain of the VCO represented as K_{VCO}. For a good phase noise performance small K_{VCO} i.e. VCO gain shall be fine but to acquire more linear FMCW chirp signal and better process-voltage-temperature (PVT) variations, a large K_{VCO} will be required to provide a wide tuning range. Therefore, a low phase noise VCO design is a challenging task for the FMCW radar system [15].

2.2 Basic Oscillator Fundamentals

Oscillators are a crucial part of the frequency synthesizers. It can be thought of as an amplifier that runs itself with the input signal through feedback. A circuit that consumes only DC power and generates a periodic AC signal at its output is called an oscillator. No input signal except for the power supply is required for the oscillations to occur.

2.2.1 Feedback Theory

A typical oscillator circuit is a negative feedback system that can be represented in Figure 4.

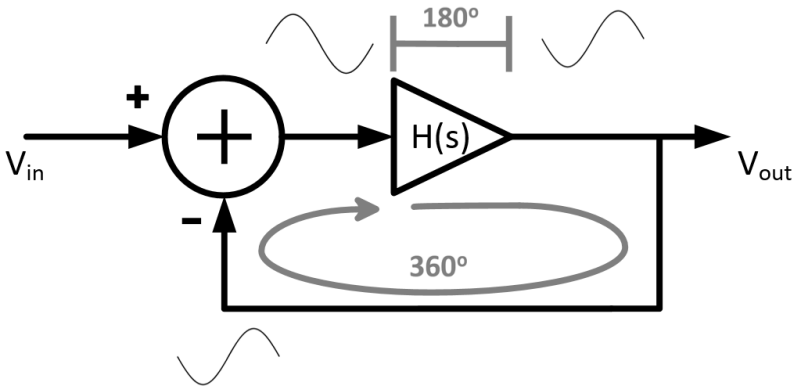


Figure 4. Negative feedback system model of an oscillator

The overall transfer function is expressed as:

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1 + H(s)}, \tag{1}$$

where the input signal $V_{in}(s)$ output signal $V_{out}(s)$ and system response $H(s)$ are the frequency domain representations. For the oscillator to maintain a steady-state of oscillations, it has to satisfy the Barkausen[16] criteria for a negative feedback system which states that:

- Magnitude criterion: The absolute value of the loop gain of the system needs to be equal or larger than unity i.e. $H(s = j\omega) \geq 1$
- Phase criterion: The frequency-dependent phase of the oscillator loop must be equal to 180° i.e. $H(s = j\omega) = 180°$. Since it is a negative feedback signal at ω will experience a total phase shift of 360° to sustain the oscillations.

These are the two necessary conditions to ensure oscillations theoretically. But in practice, these are not sufficient if only met in typical conditions. To ensure oscillations in the presence

of process, voltage and temperature (PVT) constraints, it is recommended to have an $H(s)$ two or three times the required value [17]. The Barkausen criteria apply for various feedback systems, i.e., positive or negative feedback, as shown in Figure 4 considering the total phase shift around the loop is 0^o or 360^o.

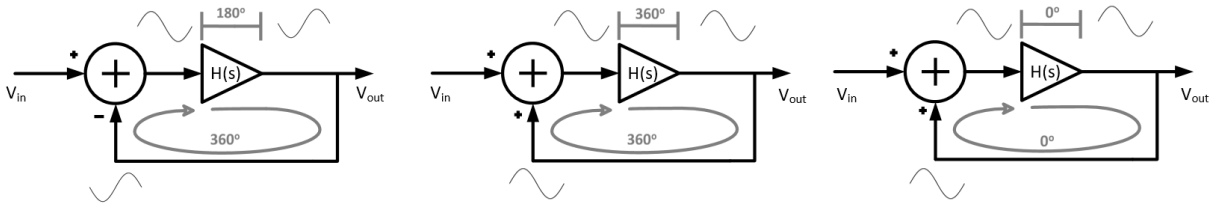


Figure 5. Negative and Positive Feedback systems

2.2.2 Negative Resistance Theory

A well-suited theory to make oscillations from the LC resonator is the negative resistance theory. A device providing negative resistance can compensate losses caused by the positive parasitic resistances. The outgoing signal power at the node where the negative resistance appears is larger than the incoming signal power. The transistors fed by a DC supply can achieve these characteristics.

To determine the oscillation frequency, a resonator is required. Either a parallel or a series connection of inductor and a capacitor is required to realize the resonator. In both cases, maximum energy is generated at the resonance frequency.

2.3 Voltage Controlled Oscillators

If the frequencies in a circuit are required to be electrically adjustable by utilizing the voltage variation, then the term oscillator is altered to voltage controlled oscillator. The VCO's are often utilized in the phase-locked loop (PLL's). A PLL is a feedback system comprised of a VCO, loop pass filter (LPF) and phase detector (PD) within its loop. The purpose is to force the VCO to lock in frequency and phase with the reference input signal. The general VCO operation can be seen from Figure 6.

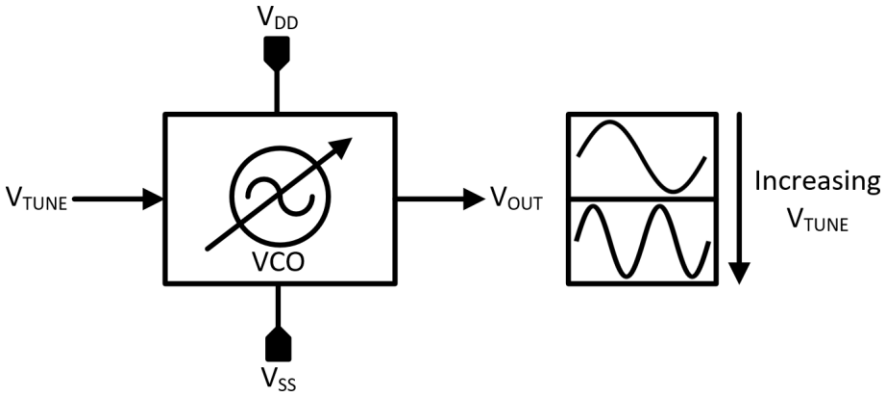


Figure 6. VCO Operation

The operation of the VCO can be justified from the equation as follows:

$$f_{VCO} = f_{center} + K_{VCO}V_{TUNE}, \quad (2)$$

where the center frequency of the VCO is f_{center} and the gain of the VCO is given by K_{VCO}. The K_{VCO} is defined as

$$K_{VCO} = \frac{\partial f_{VCO}}{\partial V_{TUNE}}, \tag{3}$$

where ∂V_{TUNE} is the variation in the input tuning voltage and ∂f_{VCO} is the change in the VCO oscillation frequency

2.3.1 VCO Characteristics

There are numerous important VCO performance characteristics a designer shall consider including the topology that shall be beneficial to meet that requirement. The general performance characteristics include center frequency, tuning range, power consumption, phase noise and jitter. Four main characteristics determine a good VCO:

1. A VCO shall be able to start and sustain oscillation over its designed frequency range PVT into account.
2. It has to meet its phase noise requirement over the bandwidth.
3. The VCO shall meet the figure of merit (FOM) specification criteria.
4. The VCO shall have a wide linear tuning range.

2.3.2 Frequency Tuning Range

An important specification for the VCO is the frequency tuning range. The highest and the lowest frequency that the oscillator can produce is defined as the tuning range of the oscillator. For mm-wave oscillation, it is usually given in GHz or as a relative number. The tuning range of the VCO can be defined as:

$$TR(\%) = \frac{\Delta f}{f_{center}} \times 100, \tag{4}$$

where TR is the tuning range, Δf = f_{max} - f_{min} and f_{center} = (f_{max} + f_{min}) /2, where f_{center} is the center frequency of oscillation, f_{min} and f_{max} are the minimum and maximum oscillation frequency and Δf is the difference between the minimum and maximum oscillation frequencies. For a fixed value of an inductor, the f_{max} and f_{min} can be determined by the maximum and minimum capacitance. Also, taking into account the fixed capacitance of the LC tank, we can modify the previous equation to:

$$TR(\%) = \frac{\sqrt{\frac{C_{vmax}}{C_{vmin}} + \frac{C_{fix}}{C_{vmin}}} - \sqrt{1 + \frac{C_{fix}}{C_{vmin}}}}{\sqrt{\frac{C_{vmax}}{C_{vmin}} + \frac{C_{fix}}{C_{vmin}}} + \sqrt{1 + \frac{C_{fix}}{C_{vmin}}}}, \tag{5}$$

where C_{vmax} and C_{vmin} are the maximum and the minimum value of the varactor capacitance. The C_{fix} is the fixed capacitance of the LC tank. It is to be noted that the parasitic capacitance of the transistors will also add up to the capacitance of LC Tank resulting in

reducing the tuning range. At mm-wave, in order to sustain the oscillations, increasing the size of the transistors will contribute to the increase of parasitic capacitance resulting in the limitation of the tuning range.

2.3.3 Power Consumption

The amount of power oscillator drains from its power supply determines power consumption over fixed supply voltage given below

$$P_{DC} = V_{DD} I_D, \tag{6}$$

where V_{DD} is DC supply voltage given in volts, I_D is the DC supply current in amperes and P_{DC} is the power consumed by the oscillator, usually in mW. In CMOS process, typically V_{DD} and I_D are utilized whereas in BJTs, V_{CC} and I_{CC} are used.

2.3.4 VCO Figure of Merit (FOM)

It is difficult to compare the performance of the VCOs as they feature different center frequencies, tuning range, power consumption P_{DC} and phase noise over offset frequencies. To compare the VCOs, a figure-of-merit in [18] was introduced. The proposed FOM did not take into account the frequency tuning range, therefore a modified $\mathrm{FOM_T}$ was presented in [19]. The latter takes into account the phase noise, frequency tuning range, center frequency and power dissipation which is given by

$$\mathrm{FOM_T} = \mathrm{PN} - 20\log\left(\frac{f_{center}}{\Delta f_{off}} \times \frac{\mathrm{TTR}}{10}\right) + 10\log\left(\frac{\mathrm{P_{DC}}}{1\mathrm{mW}}\right), \tag{7}$$

where PN is the phase noise in dBc/Hz at a frequency offset Δf_{off} and P_{DC} is the power consumption of the oscillator. TTR is the total frequency tuning range given in percentage. Higher the P_{DC}, lower is the $\mathrm{FOM_T}$ whereas the lower PN and higher TTR result in a higher $\mathrm{FOM_T}$.

2.3.5 Phase Noise and Jitter

One of the most important parameters in oscillators is phase noise and it has been extensively discussed in the literature [20][21]. An ideal oscillator generates a perfectly sinusoidal signal described as

$$V_{out}(t) = V_o \cos(2\pi f_c t), \tag{8}$$

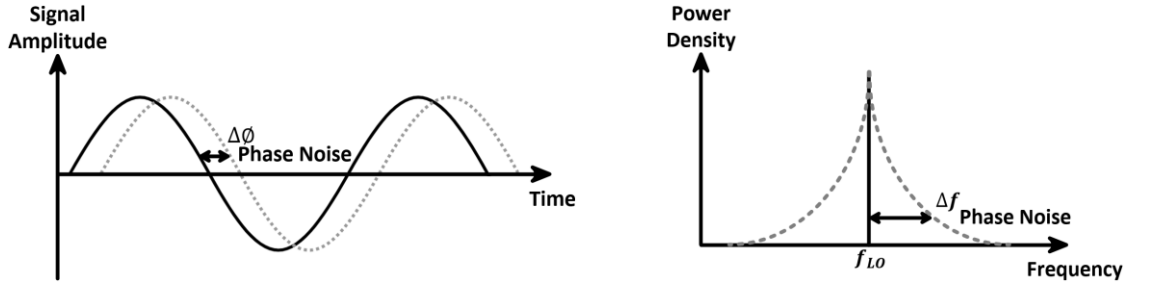
with a constant amplitude of V_o and a center frequency at f_c. In this ideal scenario, the zero crossings of the waveform occur at exactly the integer multiples of

$$T_c = \frac{2\pi}{\omega_c}, \tag{9}$$

where ω_c is the center frequency of oscillation and T_c is the time period. Practically, the zero crossing of the waveform doesn't occur at these integer multiples due to disturbances caused by the noise which can be modeled as

$$V_{out}(t) = V_o \cos\left[(2\pi f_c t) + \emptyset_n(t)\right], \tag{10}$$

where $\emptyset_n(t)$ is the disturbance that deviates the zero crossings. The fluctuations that are introduced by the $\emptyset_n(t)$ are function in the time domain result in symmetrical perturbations close to f_c in the frequency domain which can be seen in Figure 7



Time Domain Jitter (ps) *Frequency domain: Phase Noise (dBc/Hz)*

Figure 7. Jitter in time domain relates to phase noise in frequency domain

Leeson Noise Model

The noise prediction model by Leeson is based on the time-invariant properties of an oscillator, which takes into account the resonator Q, feedback gain, output power, and noise figure. It is a generally accepted method for determining the phase noise. Leeson's phase noise equation is given by

$$L(\Delta\omega) = 10\log\left[\left(\frac{2FkT}{P_{sig}}\right)\left\{\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2 + 1\right\}\left(\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} + 1\right)\right], \tag{11}$$

where $L(\Delta\omega)$ is the single sideband (SSB) noise spectral density expressed in units of dBc/Hz. T is the temperature in Kelvin, K is the Boltzmann's constant, P_{sig} is the oscillator signal power, ω_o is the oscillation frequency and $\Delta\omega$ is the offset from ω_o. The quality factor is the loaded Q of the oscillator resonator. F is the noise figure of the oscillator and $\Delta\omega_{1/f^3}$ is the corner frequency between $1/f^3$ and $1/f^2$ regions. The illustration below is the relationship of the phase noise with the frequency.

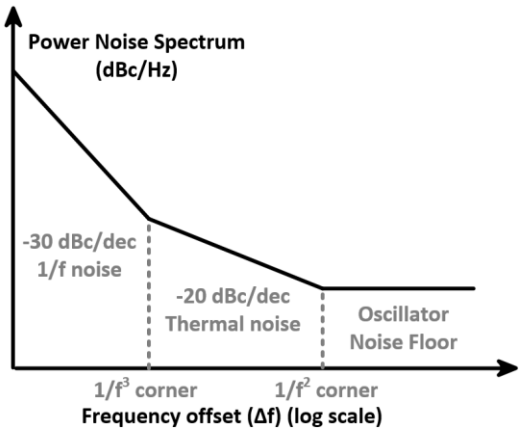


Figure 8. Illustration of phase noise versus the frequency relationship

2.4 Practical Integrated Topologies in mm-wave operation

An appropriate choice of the VCO topology is a necessity to achieve the best performance taking maximum oscillation frequency, bandwidth, output power, phase noise, and power consumption into consideration. The most common topologies used at these frequencies are Push-Push, Colpitts, and cross-coupled LC Oscillators. These are studied in the sections below.

2.4.1 Push Push VCO

High-frequency systems where the fundamental frequency of the oscillator cannot be directly employed, the harmonics of the VCO can be utilized as the output signal to acquire oscillations. The push-push oscillators are designed to produce signals at even harmonics. It consists of two symmetric sub oscillators, each one of them oscillating at half the required output frequency and has a phase difference of 180º among them. The second harmonic is extracted at the virtual ground node, where the anti-phase fundamental signals cancel out [8][22]. The spectral components of the generated signals of the sub oscillators can be represented by

$$x_1(t) = \sum_{n=1}^{\infty} a_n \sin(\omega_n + \varphi_n) \tag{12}$$

$$x_2(t) = \sum_{n=1}^{\infty} a_n \sin(\omega_n t + \varphi_n + (n+1)\pi) \tag{13}$$

Signals have the same amplitude of a_n with the difference in phase of $(n+1)\pi$, where n is the harmonic index. The output signal can be represented as the sum of the two sub-oscillator signals.

$$x(t) = x_1(t) + x_2(t) = \sum_{n=2,4,6\ldots}^{\infty} 2 \times a_n \sin(\omega_n t + \varphi_n), \tag{14}$$

The equation (14) illustrates that the fundamental and odd harmonics are cancelled out, while adding in phase the even harmonics. The power delivered to the load is at even harmonics f_2, $f_4 \ldots f_{2n}$. Figure 9 below demonstrates the concept.

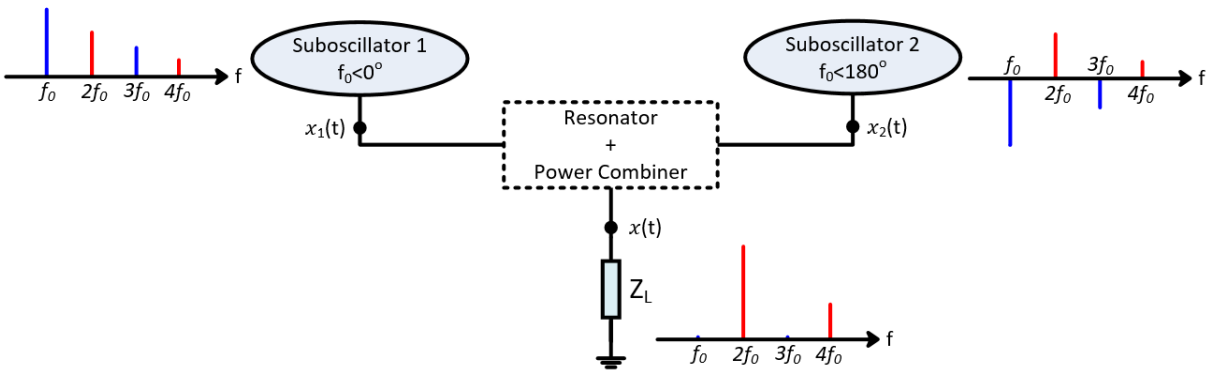


Figure 9. Push Push Oscillator Principle

2.4.2 Colpitts VCO

The Colpitts oscillator is a category of an LC Oscillator that utilizes capacitive voltage divider as its feedback source. The feedback network consists of a pair of tapped capacitors and an inductor to generate oscillations. The VCO provides a negative resistance based on the capacitive feedback [23], [24]. A single-ended Colpitts oscillator is shown in Figure 10a below. The operation can be understood by examining the resonant circuit shown in Figure 10b. The gate-drain port impedance looking into the circuit is expressed as [25]

$$Y_{eq} = \frac{-C_1 C_2 \omega^2 g_m}{{g_m}^2 + \omega^2 (C_1 + C_2)^2} + \frac{jC_1 C_2 \omega^3 (C_1 + C_2)}{{g_m}^2 + \omega^2 (C_1 + C_2)^2}, \tag{2.15}$$

where Y_{eq} is basically the equivalent negative conductance in parallel with the capacitor. C_1 and C_2 are the tapped capacitors and g_m is the transconductance of the transistor M_1. In order for the circuit to oscillate, the negative admittance has to be large enough to cancel the losses produced by the tank. Integrated circuits typically utilize the differential structures, which are shown in Figure 10c-d due to good close-in phase noise. However, they consume high power due to poor startup characteristics

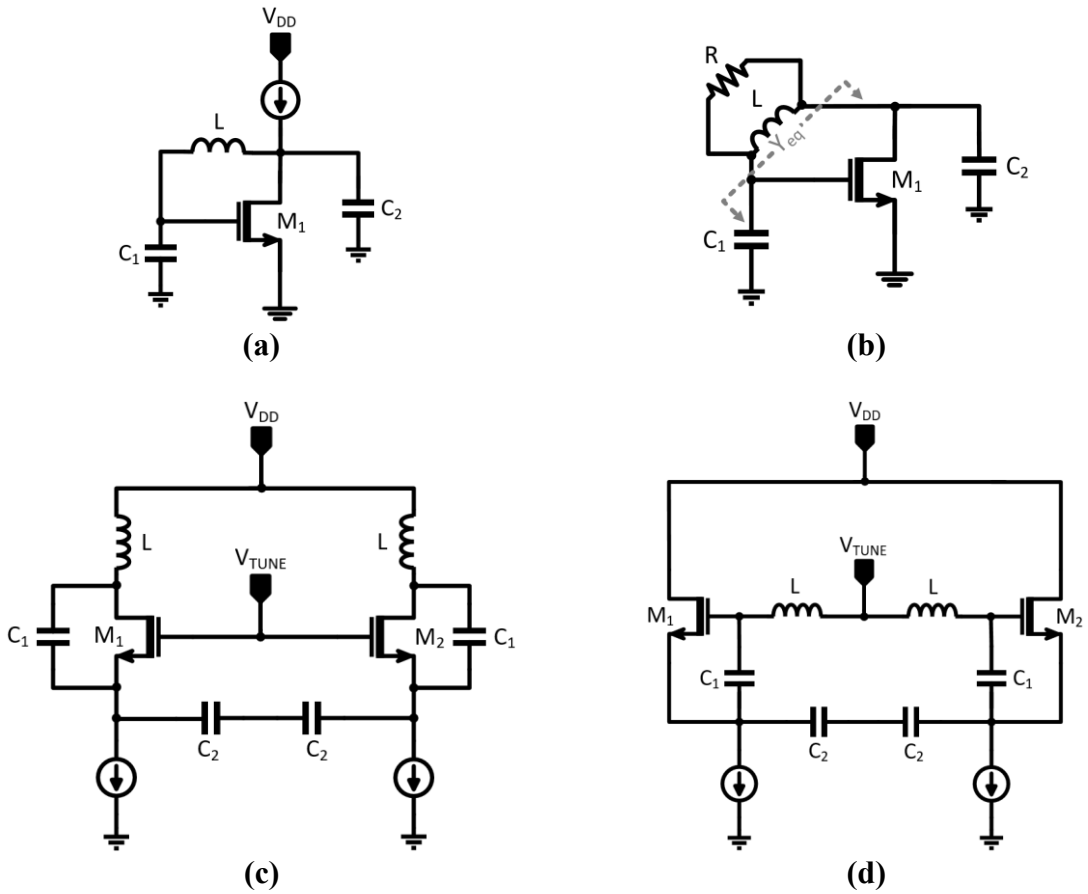
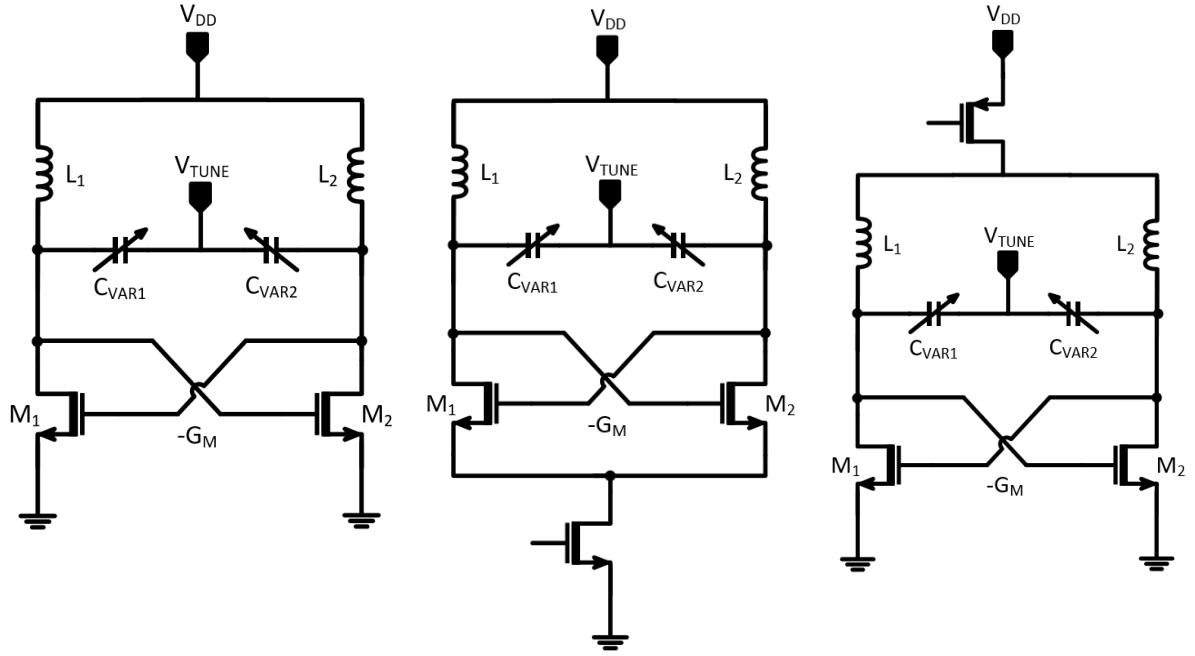


Figure 10. (a) a general Colpitts topology, (b) one port view of the Colpitts oscillator (c) differential common gate (d) differential common drain

2.4.3 Cross-Coupled LC VCO

The most popular topology for integrated radio applications is the cross-coupled LC VCO. Due to easy startup and moderate tuning range and phase noise, it is an attractive topology. The VCO of and LC tank that comprises of two inductors and a varactor. The losses of the tank, i.e., varactor, in particular, are quite high at a high-frequency range. A pair of cross-coupled pair transistors are utilized to maintain the oscillations. The transconductance of the cross-coupled pair provides negative resistance, which in turn provides energy to compensate for the losses that the produced by the LC tank. This property of the cross-coupled pair is, in fact, difficult to achieve at high frequencies due to the capacitances they contribute to the tank. Thereby in order to reach high frequencies, the size of the varactor is reduced, which leads to a lower tuning range. It is to note that the phase noise that is highly affected by the quality factor Q of the tank, which is degraded by the varactor at high frequencies. Techniques have been employed either to have a coarse tuning or fine-tuning or both for mm-wave fundamental oscillators in order to increase the frequency tuning range with low phase noise. This is achieved by employing a higher-order LC tank with dual resonant modes [26] or three resonant modes [27]. To avoid the use of low Q varactors, magnetic tuning is performed at the secondary coil by changing the current or the resistance [28][29]. Below Figure 11 demonstrates the general schematic of the cross-coupled pair implementations.



(a) (b) (c)

Figure 11. Common cross-coupled VCO Topologies

LC Tank

An ideal LC Oscillator is composed of an inductor and a capacitor. To get the oscillations to occur, it is driven with a voltage source, and the inductive reactance (X_L) and capacitive

reactance (X_C) must be equal to transfer the energy stored in the inductor and the capacitor back and forth. It will oscillate at ω_o

$$X_L = X_C \tag{16}$$

$$\omega L = \frac{1}{\omega C} \tag{17}$$

$$f_o = \frac{1}{2\pi\sqrt{LC}}, \tag{18}$$

where, f_o is the oscillation frequency.

Physically, ideal inductors and capacitors are not attainable since there are losses present in the form of parasitic series resistance R_S. The parasitic series resistance is being the most accurate, but the equivalent parallel representation R_P is usually easier to work with and is given by the transformation equation

$$Q_{ind} = \frac{\omega L_s}{R_s} = \frac{R_p}{\omega L_P} \tag{19}$$

$$Q_{var} = \frac{1}{\omega R_s C} = \omega C R_P \tag{20}$$

$$\frac{1}{Q_{tank}} = \frac{1}{Q_{ind}} + \frac{1}{Q_{var}}, \tag{21}$$

where, Q_{ind}, Q_{var} and Q_{tank} are the quality factor of the inductor, varactor, and the combined LC tank, respectively. The parallel resistance R_p is the cause of the loss in the tank and can be replenished by a negative resistance $-R_p$ to cancel the losses produced by the tank [30]. The methodology to cancel the losses is shown in Figure 12.

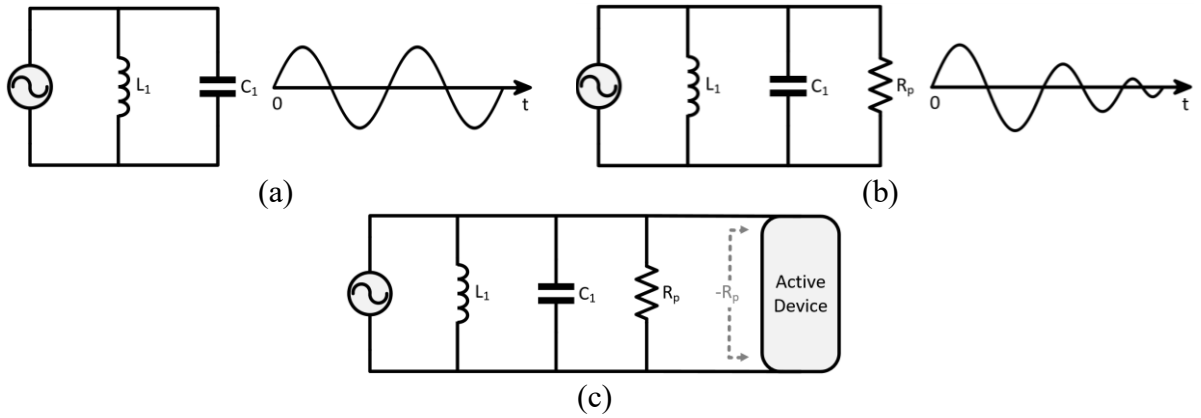


Figure 12. (a) Ideal LC Tank response, (b) Lossy LC Tank response, (c) Negative resistance (-R_P) to cancel losses of Tank (R_P)

Negative Resistance

The conventional method used to realize a negative resistance is using a cross-coupled differential pair that has an inherited property to produce negative resistance. By applying a test voltage over the cross-coupled pair, the two-port resistance between the drain nodes from Figure 13 is observed by finding i_x using superposition

$$i_x = -g_m v_x/2 + v_x/2r_{ds} \tag{22}$$

$$R_x = {}^{v_x}/_{i_x} = 2\,(-{}^{1}/_{g_m} \,||\, r_{ds}) \tag{23}$$

If $g_m r_{ds} > 1$, then:

$$R_x = -{}^{2}/_{g_m}, \tag{24}$$

thus generating a negative resistance that injects power into the LC tank, and if R_x is able to compensate for the losses, the circuit will start to oscillate. Although oscillation is a large signal behavior, the small-signal analysis provides insight into the preliminary design. Small-signal behavior is observed at the startup of the oscillator. Since the resonator is purely passive, therefore in order to satisfy the small-signal oscillation condition, the magnitude of the effective negative resistance $|R_{neg}|$ generated by the active device should be smaller than or equal to $|R_P|$ in order to compensate the losses inherent in the oscillator to achieve a steady-state.

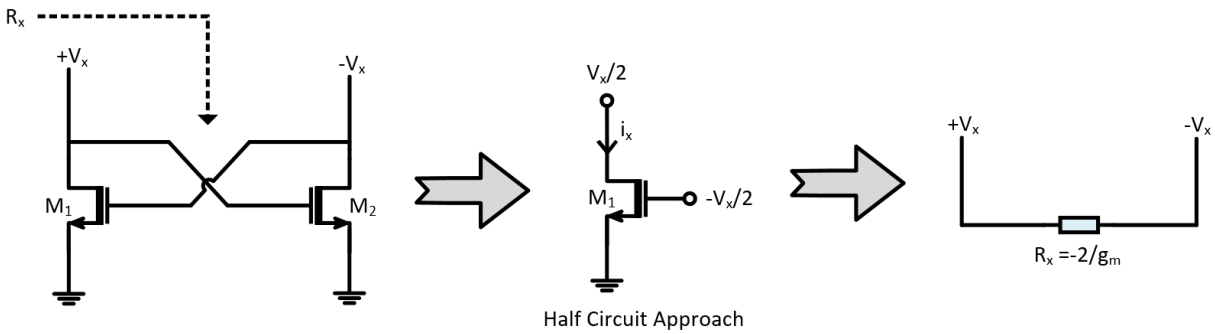


Figure 13. Differential pair modeled as negative resistance using half circuit approach

Parasitics contribution and startup

Figure 14 shows the circuit diagram of the complete VCO. To simplify the model provided in Figure 14 (a) and to grasp a more in-depth insight into the parasitic contribution by each component, Figure 14 (b) shows individual parasitics by the CCP (cross-coupled pair), varactor, inductor and the buffer stage.

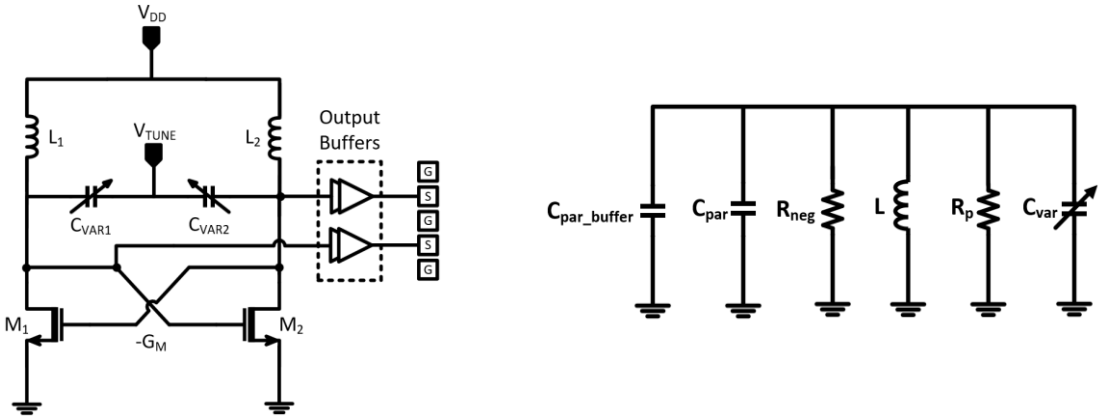
The total inductance L_T, capacitance C_T, and parasitic resistance R_P can be approximated as

$$L_T = L \tag{25}$$

$$C_T = C_{var} + C_{par} + (C_{par\_buffer} \times 2) \tag{26}$$

$$R_p = \frac{(R_{p_{var}} \times R_{p_{ind}})}{(R_{p_{var}} + R_{p_{ind}})}, \tag{27}$$

where, L_T, C_T, and R_p are the equivalent inductance, capacitance, and parallel resistance of the LC tank. C_{var} denotes the varactor capacitance, C_{par} is the cross-coupled pair parasitics whereas the parasitics associated with each buffer is indicated by C_{par_buffer}. The $R_{p_{var}}$ and $R_{p_{ind}}$ are the parallel resistance associated with the varactor and the inductor.



(a) A complete VCO circuit (b) Parasitics associated with the circuit

Figure 14. VCO and its parasitics

As explained earlier, for steady-state oscillations to occur the circuit has to satisfy the **B**arkausen criteria i.e.

- Loop gain is equal to unity.
- The phase shift around the loop is zero or an integer multiple of 2π.

The oscillation frequency (F_{osc}) and the startup condition is given by the equations [31] mentioned below, where, as mentioned earlier R_p represent the losses of the LC tank incurred by the varactor and the inductor

$$F_{osc} = \frac{1}{2\pi\sqrt{L_T C_T}} \tag{28}$$

$$G_m = \frac{g_m}{2} = \frac{1}{R_p} \tag{29}$$

To sustain the oscillations, R_{neg} produced by the G_m CCP stage shall be able to cancel the losses generated by the LC tank represented as R_p. g_m is the transconductance of a signal transistor in CCP. The selection of the inductor and the varactor determines the R_p of the LC tank. R_{neg} can be determined by taking the inverse of the G_m (transconductance) of the CCP transistors that will assist in cancelling the losses.

2.5 Passive Components

2.5.1 Accumulation-MOS Varactors

Two different tuning approaches can be implemented on a tunable LC VCO, either utilizing a variable inductance or a variable capacitance. A tunable capacitor achieves better control over the oscillator. Therefore, it is usually preferred. The name varactor comes from a variable-capacitor. In integrated circuits, three types of varactor structures are being utilized,

- PN junctions implemented in the source-drain substrate junction of a MOSFET.
- Utilizing the capacitance formed by placing the n-channel MOSFET in the n-well rather than the p-well to reduce channel resistance and to increase quality factor. Such types of a capacitor is termed as the Accumulation MOS varactors (AMOS) varactors.
- Switchable capacitors

Because the CMOS technologies have been shrinked over a decade, Accumulation MOS varactors are widely used and are the most popular ones. The acquired capacitance is the function of the voltage applied. The following figure of merits evaluates the performance of the varactor.

- capacitance ratio (C_{max}/C_{min})
- quality factor Q
- tuning characteristics i.e. (dC/dV) linearity

Figure 15 (a) shows the symbolic representation of the Accumulation MOS varactor and Figure 15 (b) shows a cross-sectional view of the NMOS varactor. For the Accumulation MOS varactors, the source and drain are n+ doped and are placed in the n-well to reduce channel resistance. The source and drain regions are shorted to apply voltage V_{TUNE} to tune the variable capacitance. The p-substrate body is grounded, and V_{GATE} is applied at the gate terminal. Figure 15 (c) depicts the small-signal model with a variable capacitor C_{var}. Variable C_{nw}, R, C_S and R_S represent the nwell to substrate diode capacitance, parasitic gate resistance, p-substrate resistance and capacitance, respectively.

The C-V characteristics of the varactor can be seen in Figure 15 (d). A small increase in the tuning range shifts the transition voltage to higher gate voltages, thereby at a fixed V_{GATE}; the V_{TUNE} tends to reduce the varactor capacitance. The tuning range of the varactor can be defined as

$$TR = {C_{max}(C_{ox})}/{C_{min}} \tag{30}$$

where C_{max} is the maximum varactor capacitance i.e. at the oxide capacitance C_{ox} and C_{min} is the minimum varactor capacitance. Taking into consideration the quality factor, an ideal varactor will be lossless with an infinite quality factor. In practice, varactors have a parasitic series resistance R_{var} and as we move to higher frequencies, the quality factor reduces shown by the equation below:

$$Q_{var} = \frac{1}{\omega C_{var} R_{var}} \tag{31}$$

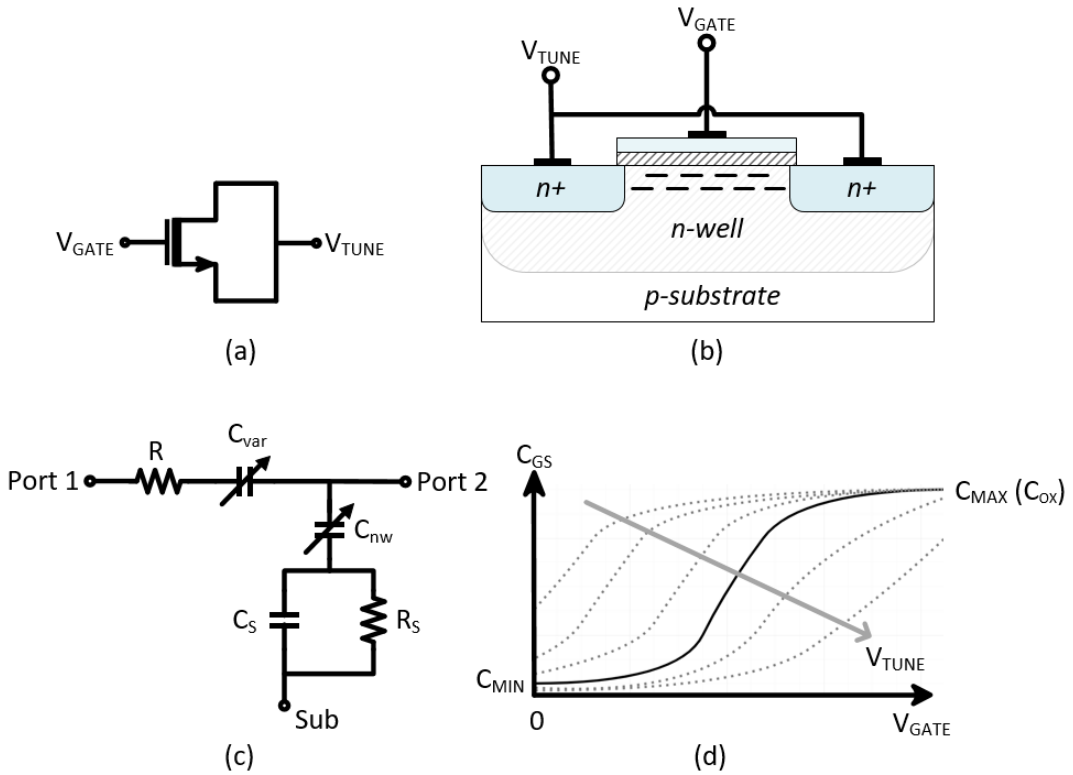


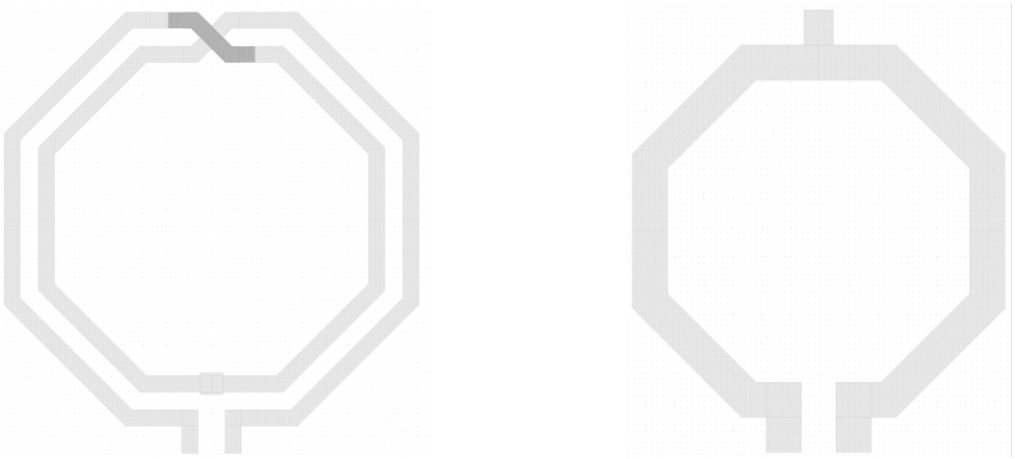
Figure 15. (a) accumulation MOS Varactor symbol (b) cross-section of a typical accumulation MOS varactor (c) simplified small-signal equivalent circuit (d) CV characteristics of accumulation MOS varactor

2.5.2 Inductors

Symmetrical inductors are widely used in oscillator designs. They exhibit high-quality factor (Q) with the benefit of reduction in phase noise than the asymmetrical topologies if they are driven differentially [32]. In practice, Inductors are realized in an octagonal shape to minimize series resistance for a given inductance. Three attributes shall be reflected in an inductor model

- inductance value
- parasitic capacitance surrounding the structure (i.e. self-resonance)
- quality factor

Driving one inductor differentially instead of utilized two single-coil inductors assists in the overall inductance per area, exploiting the coupling factor leading to higher inductance to parasitic capacitance (L/C) ratio. This technique effectively aids the differential Q to reach high frequencies.



(a) (b)

Figure 16. (a) a 2-turn symmetric Inductor (b) a single turn symmetric Inductor

2.6 Buffers

To measure the VCO, the high output impedance of the VCO core shall be converted to 50 Ω load matched, and this is achieved by the buffers. The oscillator output voltage swing shall be high enough to drive the following stage. A buffer is required to deliver the needed amount of amplitude to the load. The loaded capacitance shall reduce the oscillation frequency and the frequency tuning range. The phase noise shall also be affected by the load. The two transistor configurations mostly used as buffers for the VCO are source followers and common source (CS) amplifiers.

2.6.1 Source Follower

The common drain stage as source follower has a relatively high input impedance and a low output impedance, therefore, making it suitable to drive a 50 Ω load. This is the reason source follower is a good buffer candidate. The typical examples of the source follower buffer can be seen in 80 GHz Voltage Controlled Oscillator [6] and the design of a 77 GHz LC-VCO with a slow-wave coplanar stripline-based inductor [33]. Figure 17 shows a buffer schematic utilizing the source follower configuration. The M_1 and M_2 transistors are dimensioned with respect to 50 Ω load that shall be connected to the S+ and the S- terminals. The differential transmission line TL_2 is matched to the output load. The TL_2 length is matched to 50 Ω. It is adjusted to be around λ/4 to make an open circuit at the oscillation frequency f_0 and to cancel the imaginary part seen at the output. The differential transmission line TL_1 is adjusted to be around λ/4 to make an open circuit for the signal not to pass through the supply and also assisting in the reduction of buffer loaded capacitance.

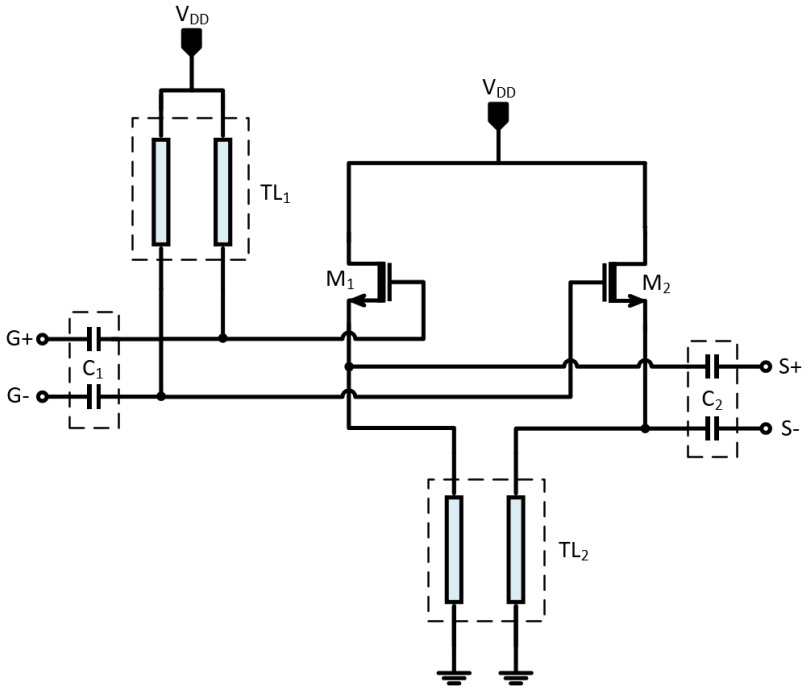


Figure 17. Source follower buffer schematic

2.6.2 Common Source

The common source acts as a voltage-controlled current source, which converts the input voltage to the current. The current is then converter back to voltage in the load. Implemented in 118 GHz fundamental VCO in [9] utilizing the common source configuration with a slight tweak in the design. To provide a shield to the VCO core, and the variation of the output impedance, the gate to drain capacitance (C_{GD}) was being neutralized by implementing the neutralization technique. The neutralization will ensure the stability of the differential amplifier with conjugate matching. Figure 19 demonstrates the buffer schematic diagram, buffer transistors M_1 and M_2 are matched to the output load using a parallel differential transmission line TL_2. To decouple the DC from the probes, the series capacitor C_2 is being used. Similarly, to decouple the DC operating point of the oscillator core from the buffer input, the series capacitor C_1 is utilized. The TL_1 is tuned to reduce the input loaded capacitance. Its length shall be close to $\lambda/4$ to create a high impedance towards so that the signal can comfortably pass through the transistor M_1 and M_2 easily instead of going into the biasing circuitry. The 50 Ω load is connected to the D+ and the D- terminals.

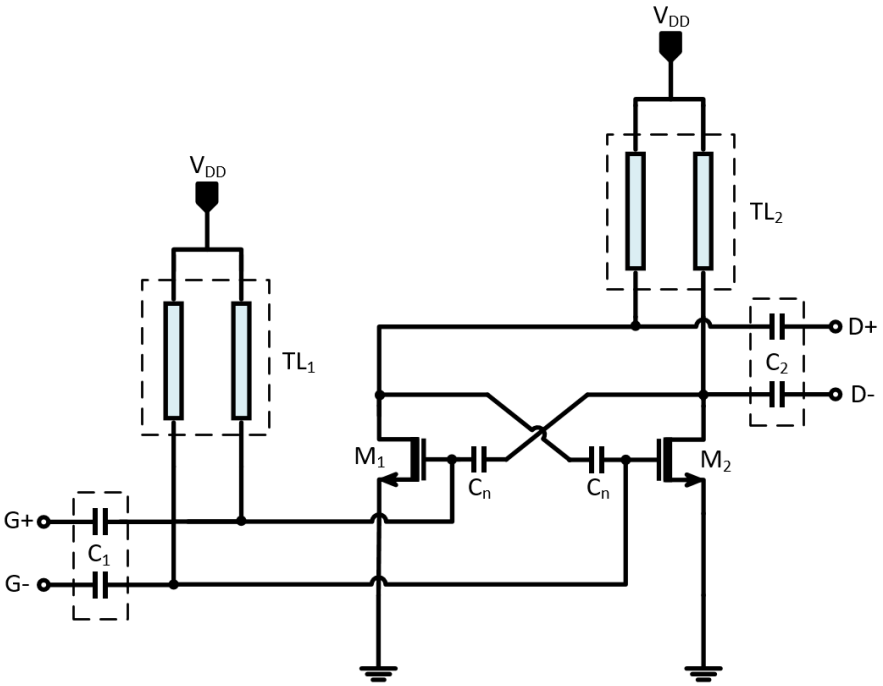
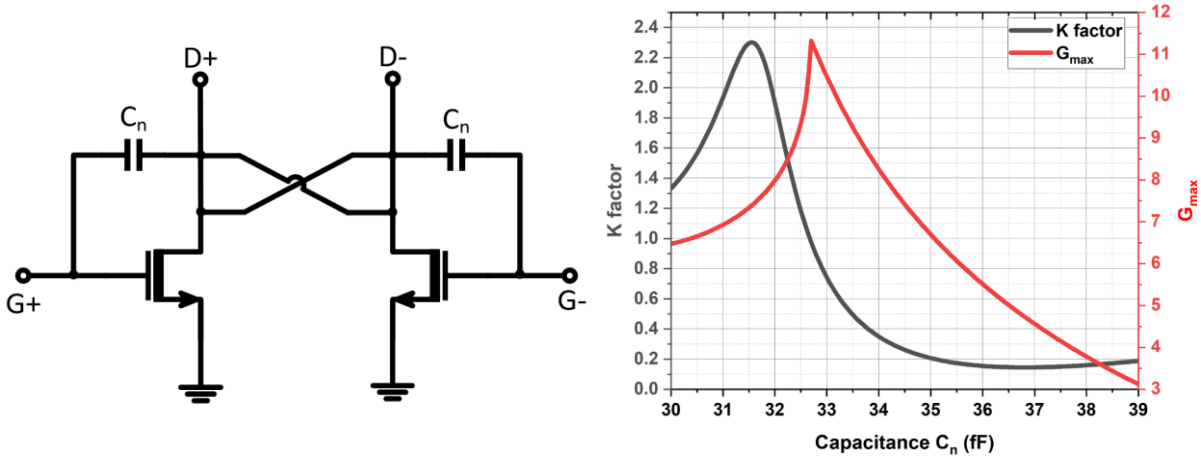


Figure 18. Common source buffer schematic with capacitive neutralization

Neutralization Technique for differential pair

This technique has been widely exercised to stabilize the amplifier without compromising the gain of the transistors [34]. It works by using a pair of cross-connected capacitors C_n in a differential pair amplifier, and these neutralization capacitors C_n will introduce an equivalent capacitance $-C_n$ that compensates the inherent capacitance C_{GD} of the transistor, thus neutralizing it. This technique is useful to achieve higher maximum power gain (MAG, also known as G_{max}) and stability (K factor). To obtain the value of the neutralization capacitor C_n, the K factor and the G_{max} are plotted as a function of the C_n at the frequency of Interest. K peaks when C_n equals C_{GD} and its larger than 1, satisfying the unconditional stability criteria. The stability of the transistors is guaranteed at this frequency, where the K factor peaks. Figure 19 demonstrates the behaviour.



(a) Schematic implementation for neutralization

(b) K factor and maximum power gain for neutralization

Figure 19. Neutralization technique for differential pair

3 LC TANK VOLTAGE CONTROLLED OSCILLATOR DESIGN

As discussed in Chapter 2, several VCO design issues and solutions have been reported. In this thesis, all VCO variants are based on the conventional LC VCO topology. In earlier discussions, improvement in VCO performance in terms of phase noise, tuning range and power consumption is tricky to achieve. This is due to the varactor quality factor that degrades at high frequencies. For inductors, symmetric high Q Inductors are a better option to begin with, as those are relatively easy to design.

In this chapter, we deal with the conventional LC VCO topology. The chapter clarifies the objectives, methodology of the design, characteristics of the varactor and the inductor, cross-coupled pair design, and the output buffer design.

3.1 Objectives

The objective of the thesis work is to design a D-band VCO for radar applications that have an acceptable frequency tuning range for the center frequency. The potential of an LC fundamental oscillator to able to reach these frequencies and ultimately, a prototype model is constructed. To simulate the VCO using the industry-standard Cadence Virtuoso program is being used. Specifically, the design targets for the VCO are:

1. Design a D-band Voltage Controlled Oscillator (VCO) for radar applications.
    a. Utilize LC VCO fundamental topology
    b. Maximize tuning range within the limits of technology
    c. Acceptable phase noise (-80 dBc/Hz at 1MHz and -104 dBc/Hz for 10 MHz)
    d. The signal output power of -5dBm
    e. Low power consumption

3.2 Methodology

An LC VCO topology is usually preferred in the VCO topologies due to its relatively low phase noise performance. As shown in Figure 20, The LC VCO tank consists of cross-coupled transistors M_0 and M_1 cross-coupled transistors that generate negative resistance i.e. $R_{neg} = 2/g_m$, to compensate the losses added by the LC tank. In order to tune the oscillators, two varactors C_{var1} and C_{var2} are employed. Center tapped inductor L_1 and L_2 are represented in a similar manner. For the output matching to the 50 Ω, buffers are utilized. The loaded capacitance of the buffer is reduced to minimize the loading effect on the oscillator. The details were described earlier in Section 2.4.3.

At mm-wave and specially D-band frequencies, it is challenging to generate sufficient negative resistance to compensate for the losses that are produced by the LC tank. The dimensioning of the inductance and the CCP is crucial since the G_m CCP stage will add its parasitic capacitance C_{par} in the circuit, thus lowering the oscillation frequency (F_{osc}). The W/L ratio of the transistors in G_m CCP stage is carefully chosen to provide sufficient negative resistance ($2/g_m$) with low parasitic capacitance. The characteristics of the varactor selection and inductor selection is being explained in the forthcoming sections.

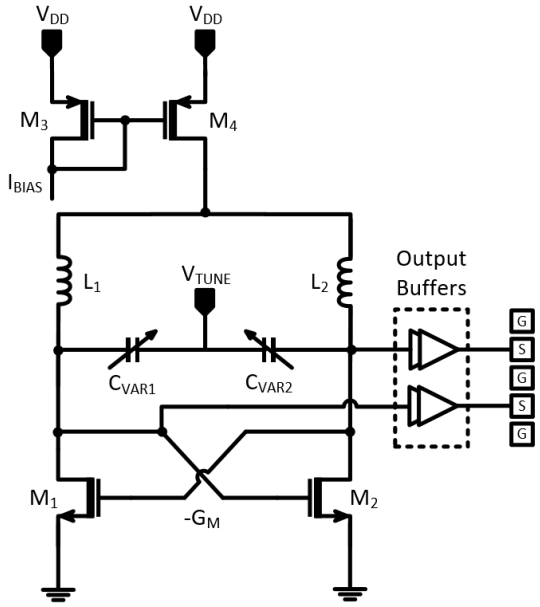


Figure 20. Schematic of the LC VCO design

The design methodology of the VCO in the 22nm SOI process has various trade-offs with the selection of varactor, inductor, G_m of CCP stage to have a compromise between the performance parameters. The quality factor of the LC tank is the most critical parameter since it can lead to high power consumption and degradation of tuning range and phase noise. The design procedure goes through a series of steps that are explained below:

(a) For the desired oscillation frequency (F_{osc}), i.e., 150 GHz, the inductance and capacitance are fixed, and the tank is optimized for a maximum quality factor.
(b) R_p is determined that will assist in finding R_{neg} and eventually C_{par} is known.
(c) The G_m CCP stage is designed to generate the required R_{neg} at a minimum C_{par}.
(d) The tank capacitance and inductance are optimized to generate the required oscillation frequency (F_{osc}).

Before proceeding to the methodology mentioned above, the Individual components will be studied, and their characteristics are needed to be determined in the 22nm SOI process.

3.2.1 Characteristics of inductor and varactor in 22nm CMOS SOI technology

In this section, we will observe the characteristics of the inductor and the varactor available in the 22nm process node. The inductor and the varactor are the schematic (library) components available at this process node. The simulations in this section are carried out at 150 GHz.

Characteristics of the inductor

As discussed earlier, since we have selected the conventional LC VCO topology, a study of the differential inductor provided by the technology is necessary. Figure 21 illustrates the layout of a differential symmetric inductor. The inductor is dc biased at 0.8V. As seen from the figure, the inductor can be characterized by two variables, i.e., the width of the coil (W) and the inner diameter (D).

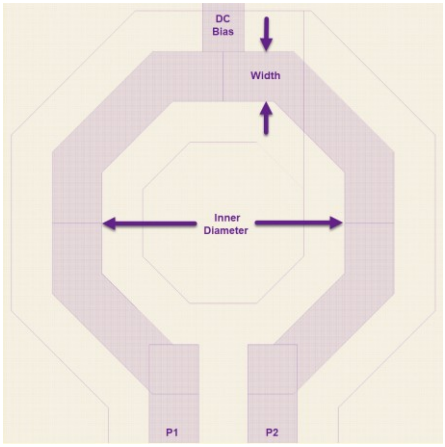
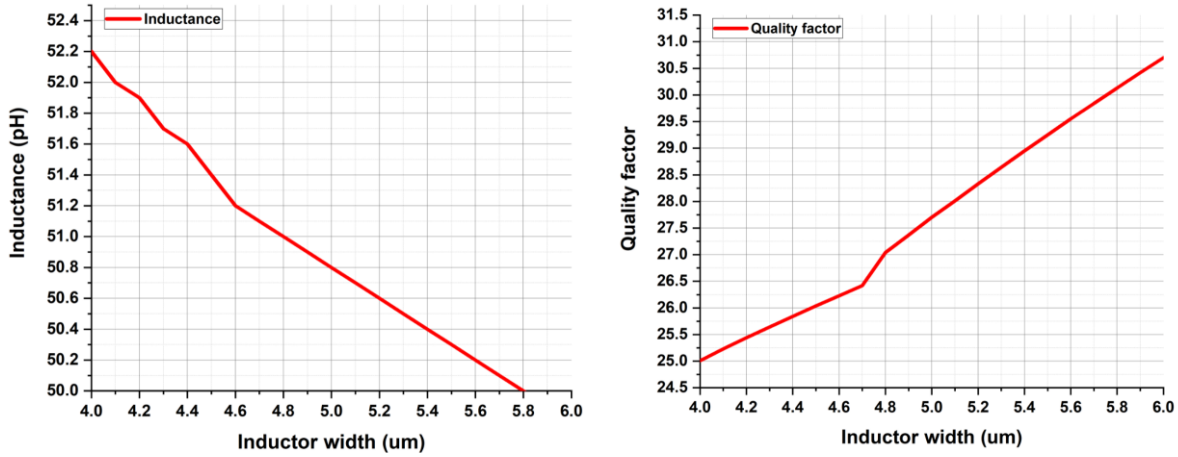


Figure 21. Layout view of the differential symmetric inductor

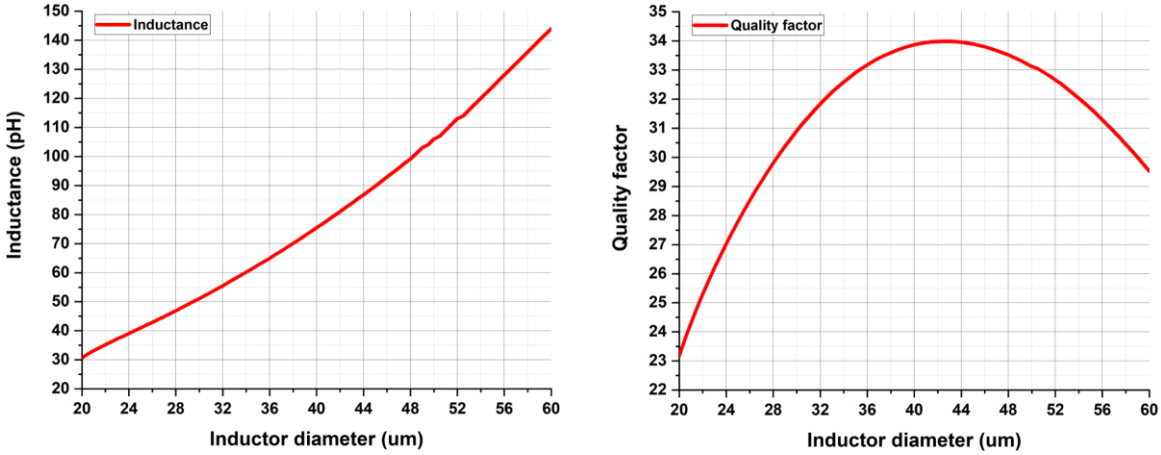
Figure 22 demonstrates the variation of the width effect on the inductance and the quality factor. It is to be noted that this technology allows the coil width to have a variation from 4 µm to 6 µm, and the inner diameter has a variation from 20 µm to 80 µm. In this scenario, the diameter was kept constant at 29.6 µm. As seen from Figure 22(a), with the increase in coil width, the inductance value is reduced due to the reduction in the area of the coil resulting in the reduction of the magnetic field in the loop. On the other hand, an increase in coil width results to decrease in the series resistance, thus improving the quality factor, as seen from the Figure 22(b). Thereby, to obtain a high Q inductor, a 6 µm width shall be chosen.



(a) inductance vs. inductor width (b) quality factor vs. inductor width

Figure 22. Effect of the variation of Inductor width

Figure 7 demonstrates the variation of the inductor inner diameter on the inductance and the quality factor. It is to note here that the width was kept constant at 6µm. As seen from the Figure 7(a) with the increase in coil diameter, the area of the coil is increased, the magnetic flux grows accordingly, thereby resulting in an increase in the inductance value. Whereas the quality factor peaks at 42 µm with the increase in diameter, and then it declines. Therefore, in order to achieve a decent quality factor of 30 above, the inner diameter of the inductor shall be higher than 28 µm and less than 42 µm.



(a) inductance vs. variation of the inductor diameter

(b) quality factor vs. variation of the inductor width

Figure 23. Effect of the variation of Inductor diameter on performance

Characteristics of the Varactor

The 22nm CMOS SOI has a very low V_t transistor-based varactor available. In addition to the library varactor, the conventional transistors can be used to act as a varactor by shorting the drain and the source terminals. This section will demonstrate the performance comparison of different types of varactors and will aid in the selection process of a suitable varactor for the LC VCO oscillator. Table below gives an overview of the options available for the varactor.

Table 1. Varactor library component options available

No.	Varactor Options
1	Built-in library varactor
2	Thin oxide transistor
3	Thick oxide transistor

To compare the performance of these different options available. Simulation setup in Figure 24 was being utilized for the varactor. Y parameters were used to extract the capacitance and the quality factor. The drain and source terminals are combined for transistor-based components. The built-in varactor source and drain terminals are combined in the library layout itself. The capacitance and the quality factor can be given as

$$C = \frac{1}{\omega * Im(Y_{12} + Y_{21})/2}, \tag{32}$$

$$Q = \frac{Im\,(Y_{11})}{Re\,(Y_{11})} \tag{33}$$

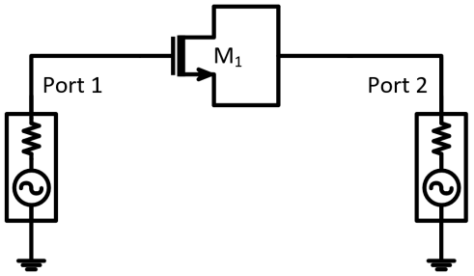
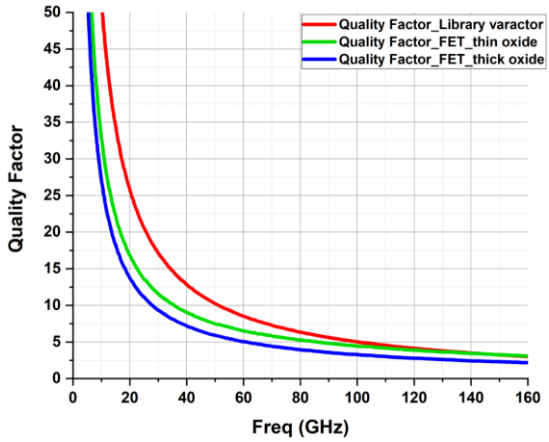
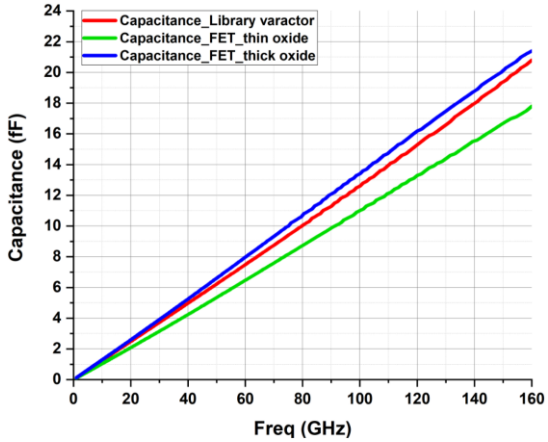


Figure 24. Simulation Setup for varactor

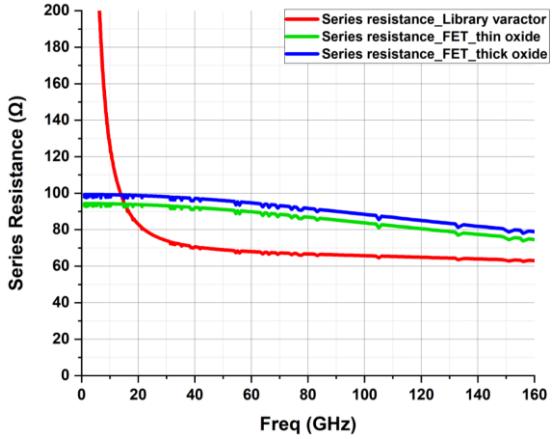
Figure 25 exhibits the quality factor, capacitance and series resistance comparisons of the aforementioned varactors over the frequency range from 1 GHz to 160 GHz at a fixed V_{tune} voltage of 0V. The transistors were simulated to have the same width of 30 µm and a channel length of 100 nm. Figure 25 (a) verifies the equation (31) presented in Section 2.5.1 for the quality factor to be dependent on frequency, capacitance and the series resistance. With the increase in the frequency, the quality factor is degraded. On the other hand, the varactor capacitance C_{var} is increased as seen from the Figure 25(b) thus also contributing in the degradation of the quality factor whereas the series resistance is decreased with the increase in the frequency as depicted in Figure 25(c). From the three plots presented in Figure 25, it is observed library varactor performs better in terms of the quality factor and the series resistance. While on the contrary, thick oxide FET outperforms the library varactor in terms of capacitance.



(a) Quality factor vs frequency



(b) Capacitance vs frequency



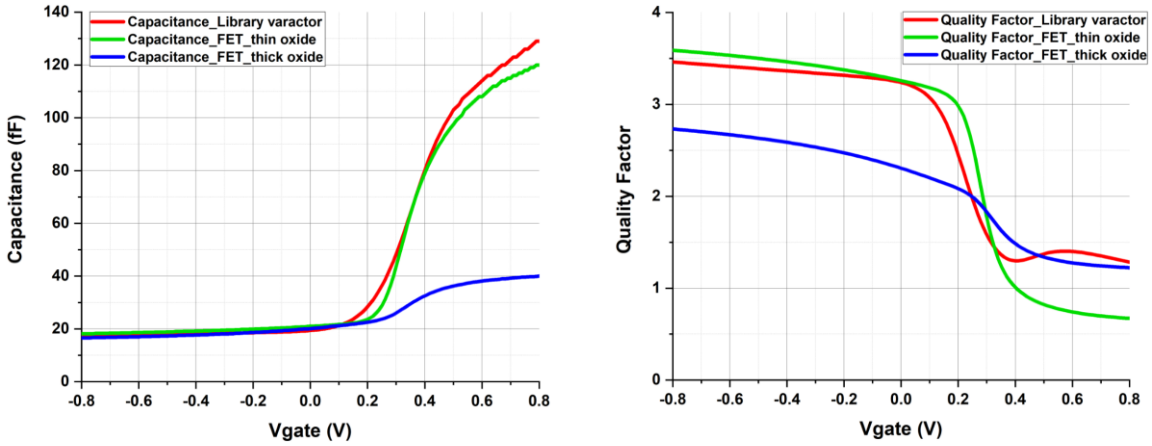
(c) Series resistance vs frequency

Figure 25. Performance parameters comparison of the transistors over the frequency

Furthermore, to have a fair comparison between all the possible varactor options over a specified voltage range. Two different comparison are made at the same frequency i.e. 150 GHz:

- At the same transistor size.
- At the same capacitance C_{max} value.

The voltage is swept from -0.8V to 0.8V and different parameters were observed, i.e., C_{max}, C_{min}, quality factor, series resistance and capacitance tuning range. Figure 26 depicts the comparison of capacitance and quality factor generated by the varactor. A detailed comparison can be seen from Table 2.



(a) Capacitance vs. Gate Voltage (b) Quality factor vs. Gate Voltage

Figure 26. Capacitance and Quality factor comparison for the same transistor widths

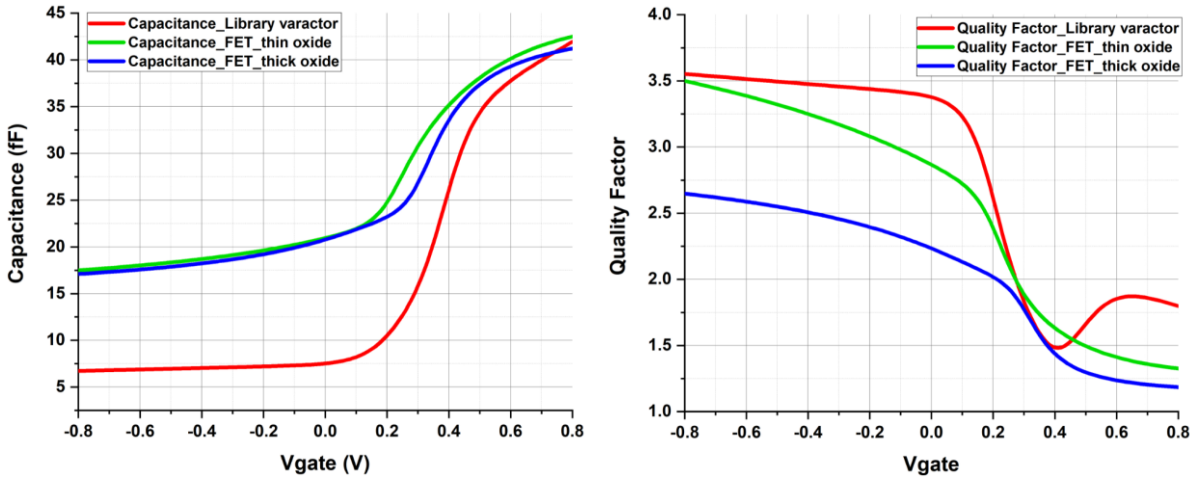
As seen from Figure 26 and Table 2, for an identical transistor width, the library varactor generates a higher capacitance value when swept over the voltage range, which can be seen in the tabular representation by the difference of C_{max} and C_{min}. Also, offering a higher capacitance tuning range. The overall Q factor throughout the swept range shall be higher than others, which can be seen by the library varactor. The comparison results make library varactor a prominent choice amongst others while selecting the varactor with equal transistor widths

Table 2. Performance comparison of all varactor options at same transistor width

Parameters	**Varactor**		
	Library varactor	**FET_thin oxide**	**FET_thick oxide**
C_{max} (fF)	128.88	119.65	39.92
C_{min} (fF)	17.23	18.14	16.56
C_{max} - C_{min} (fF)	111.64	101.5	23.353
Q @ C_{max}	1.28	0.67	1.22
Q @ C_{min}	3.46	3.58	2.73
Q (Avg)	2.37	2.13	1.97
Tuning Range (%)	7.49	6.6	2.41
Series Resistance (Ω)	63	81	76

After concluding with the first test of the performance comparison, varactors were dimensioned to match the C_{max} capacitance value to approximately 42 fF, and the corresponding performance parameters were observed. In order to obtain the same capacitance C_{max} value

from the transistors, they were dimensioned accordingly. The comparison results are demonstrated in Figure 27 whereas the detailed comparison is illustrated in Table 3.



(a) Capacitance vs. Gate Voltage (b) Quality factor vs. Gate Voltage

Figure 27. Capacitance and Quality factor comparison for the same Cmax value

It can be seen that the library varactor outperforms other varactors to have a wide variation in minimum and maximum capacitance value i.e. C_{max} and C_{min}, thus assisting in the higher capacitance tuning range as compared to others. Apart from its high tuning range, it also demonstrates a better quality factor over the voltage variation. The library varactor depicts better performance at the expense of significant series resistance due to the smaller width of the varactor.

To conclude, the library varactor is performing better in all the tests performed above, with very few demerits as compared to others. The library varactor is a foundry optimized varactor and is taken forward in the further design process.

Table 3. Performance Comparison of all varactor options at the same C_{max} value

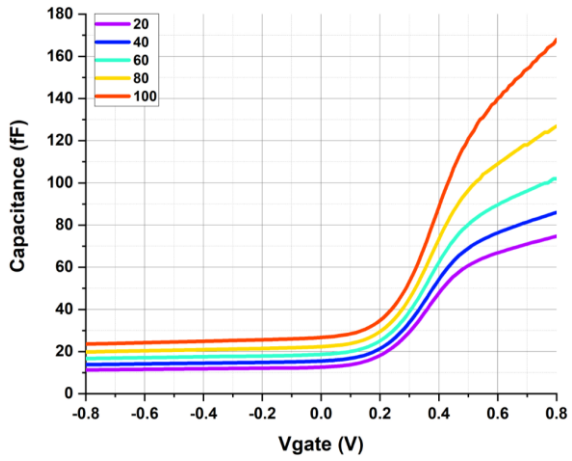
Parameters	Varactor		
	Library varactor	FET_thin oxide	FET_thick oxide
C_{max} (fF)	41.94	42.5	41.21
C_{min} (fF)	6.73	17.49	17.1
C_{max} - C_{min} (fF)	35.21	25.01	24.11
Q @ C_{max}	1.8	1.33	1.19
Q @ C_{min}	3.55	3.5	2.65
Q (Avg)	2.68	2.41	1.92
Tuning Range (%)	6.23	2.43	2.41
Series Resistance (Ω)	120	110	75

Library varactor Characterization

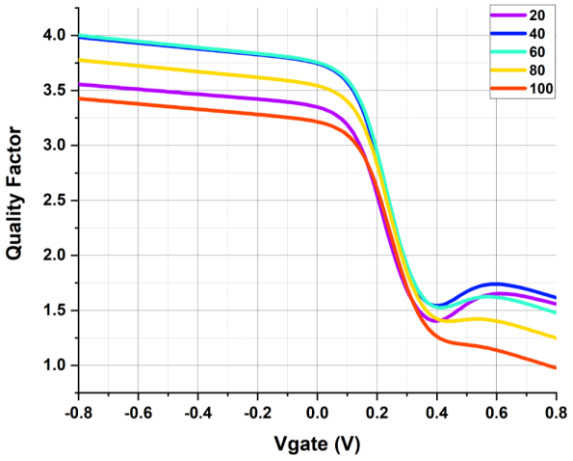
To study the selected varactor, we need to characterize some design parameters associated to the varactor to acquire the optimum performance. Finger width (W) and channel length (L) have effects on the varactor with a voltage tuning range from -0.8 to 0.8V. Figure 28 shows the variation of the finger width (W) when the size of the device is kept constant. It can be seen in Figure 28(a), increasing the number of fingers increases the capacitance, thereby experiencing

a higher tuning range as depicted in Figure 28(c). In contrast, the quality factor is degraded due to larger series resistance shown in Figure 28(b) and (d). Selecting a transistor of the same width with a lower number of fingers and a high finger width reduces the tuning range but has the benefit of a good Q factor over the voltage range.

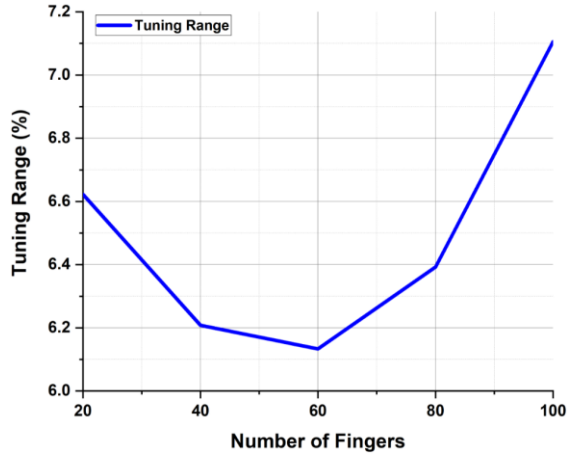
From Figure 28, we can observe a trade-off between the capacitance and the quality factor, and the tuning range variation is from 6.6% to 7.1%. The quality factor is a major concern at these operating frequencies, therefore, keeping in mind the trade-offs, the varactor dimension of with number of fingers of 40 seems to a better choice that depicts a better quality factor and a decent tuning range of 6.2%



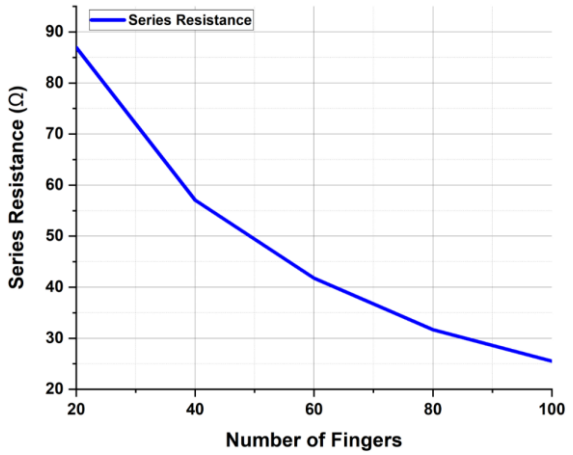
(a) Capacitance vs. Gate Voltage



(b) Quality factor vs. Gate Voltage



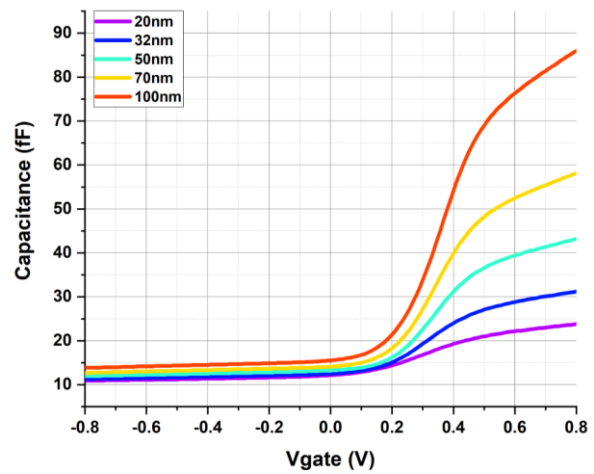
(c) Number of fingers vs. Tuning Range



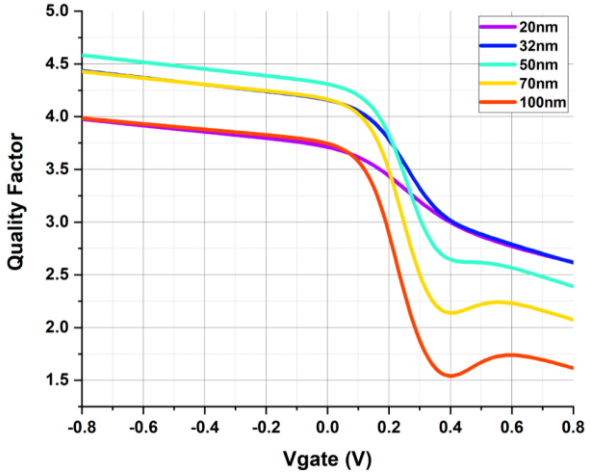
(d) Number of fingers vs. series resistance

Figure 28. Capacitance and quality factor comparison at different finger widths

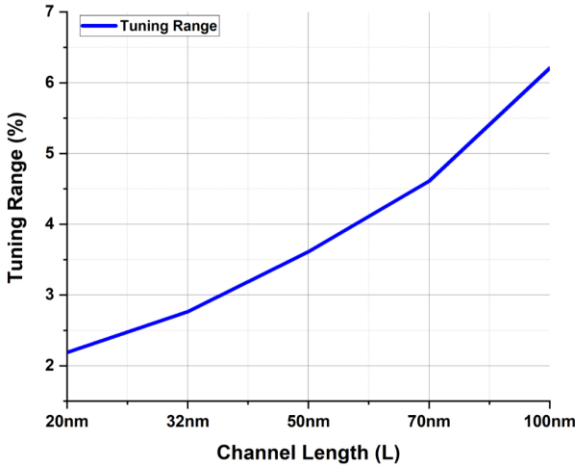
Figure 29 depicts the characteristic of the varactor for the variation in the channel length at 20, 32, 50, 70, and 100 nm, respectively. The width of the fingers was kept constant for these sets of simulations. Figure 29(a) shows an increase in the capacitance as the channel length is increased, offering a higher tuning range. The channel length of 20, 32 and 50 nm shows a better quality factor as compared to 100 nm and 70 nm. As discussed earlier, there is always a trade-off between the tuning range and the quality factor. In this set of simulations, the tuning range of 6.2% has an advantage over the quality factor thereby, 100nm channel length was considered to be a better choice.



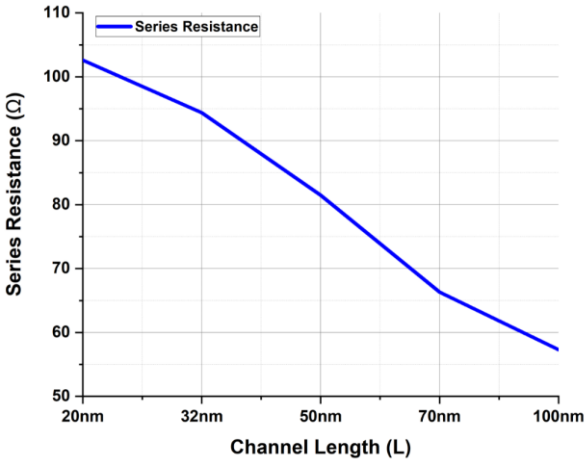
(a) Capacitance vs. Gate Voltage



(b) Quality factor vs. Gate Voltage



(c) Channel length vs. Tuning Range

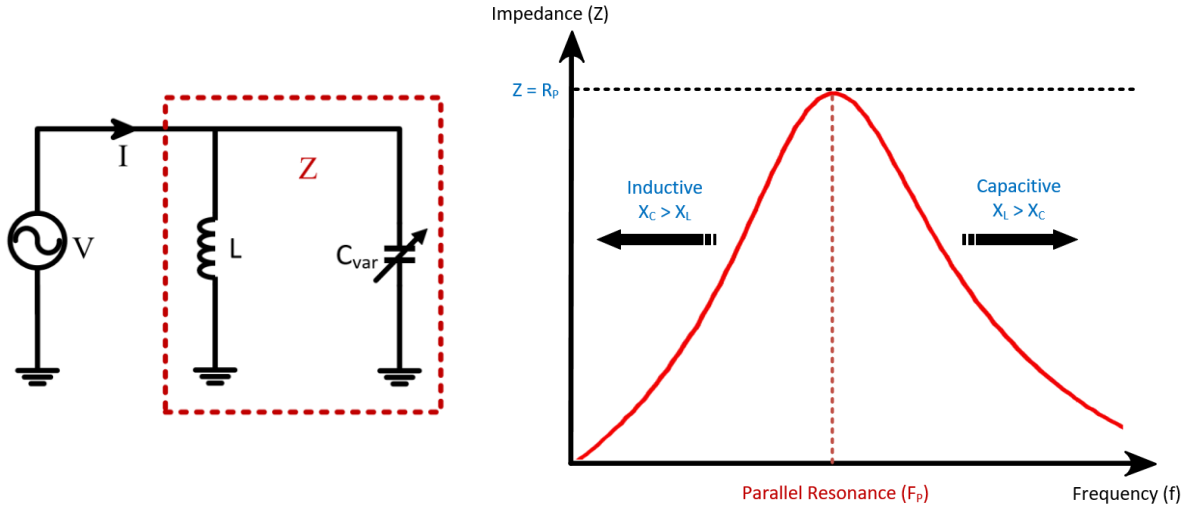


(d) Channel length vs. Series resistance

Figure 29. Capacitance and quality factor comparison at different channel lengths

3.2.2 LC Tank Characterization

The LC tank of the VCO is characterized by estimating the equivalent parallel resistive losses (i.e., R_p) produced by the tank. This is achieved by combining the LC tank in the circuitry and obtaining the impedance vs. the frequency plot. The frequency at which the resonance has the highest peak is the parallel resonance frequency where the phase of the imaginary part cancels out, and we are only left with the real part of the impedance, which is the parallel resistance (R_p). The next section will discuss the negative G_m stage that will assist to compensate for the losses produced by the LC Tank.



(a) Simulation Setup (b) Parallel Resonance of the circuit

Figure 30. Parallel resistance extraction

3.2.3 NMOS Cross coupled pair G_m stage

As discussed earlier, the LC tank loss is compensated by an active G_m CCP stage. It is to be kept in mind that the CCP adds its parasitic capacitance (C_{par}), which is big enough to lower the oscillation frequency and to reduce the tuning range of the oscillator.

NMOS cross-coupled pair G_m stage Characterization

The CCP stage is characterized to achieve maximum transconductance (G_m) of the CCP stage from a transistor. To achieve this, two sets of simulations are conducted, the first set of simulations concerns the finger-width (fw), and the second set of simulations is for the channel length (L). The parameters are swept at different transistor sizes to find the optimum transistor size. The figure below shows the schematic of the NMOS cross-coupled pair G_m stage and its simulation setup.

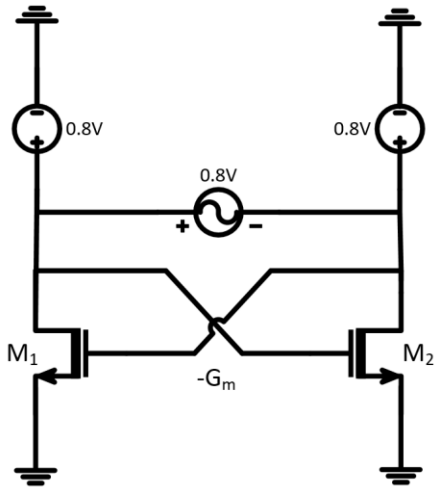


Figure 31. Simulation Setup for G_m CCP stage characterization

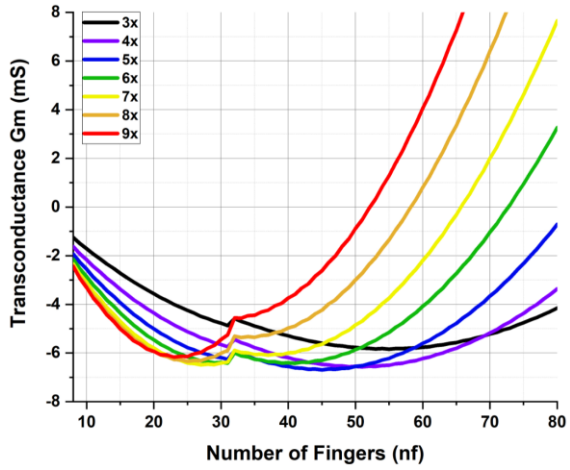
The CCP is biased at 0.8V DC which is the maximum voltage the transistor operates in this process, and AC signal is fed differentially to calculate the G_m, capacitance (C_{par}) and negative resistance (R_{neg}) as shown below from the equations:

$$G_m = real\left(\frac{I}{V}\right) \tag{34}$$

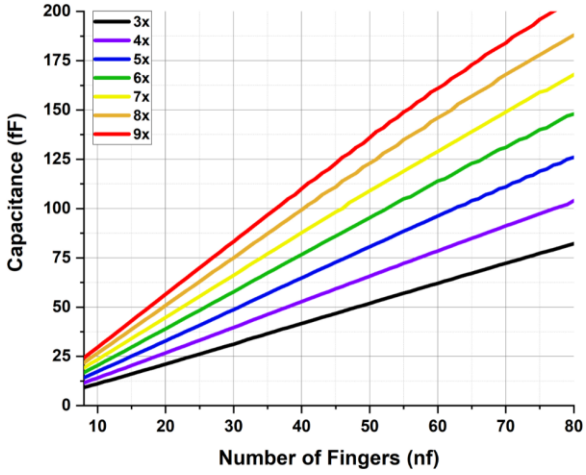
$$\mathrm{R_{neg}} = \frac{1}{G_m} \tag{35}$$

$$C_{par} = \frac{imag\left(\frac{I}{V}\right)}{2\pi f} \tag{36}$$

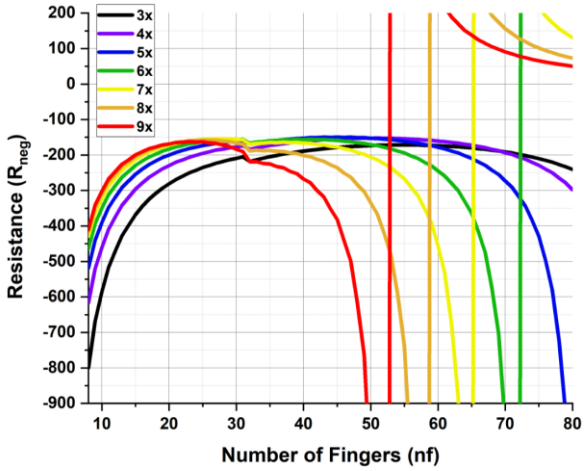
Figure 32 represents the comparison of different parameters at different relative finger-widths. The channel length of the transistor was kept at 20nm constant. From Figure 32(a), the 700 nm transistor achieves the maximum G_m of 6.43 mS at 26 fingers with a capacitance of 56.75 fF in Figure 32(b), producing a negative resistance of -155.6 Ω at 26 fingers as seen in Figure 32(c). The 7x transistor provides a change of negative resistance from -420 Ω to -155.6 Ω. Although 7x has a higher parasitic capacitance value as compared to others but it benefits with high G_m and low R_{neg}, thereby making it a suitable option.



(a) Number of fingers vs. transconductance G_m



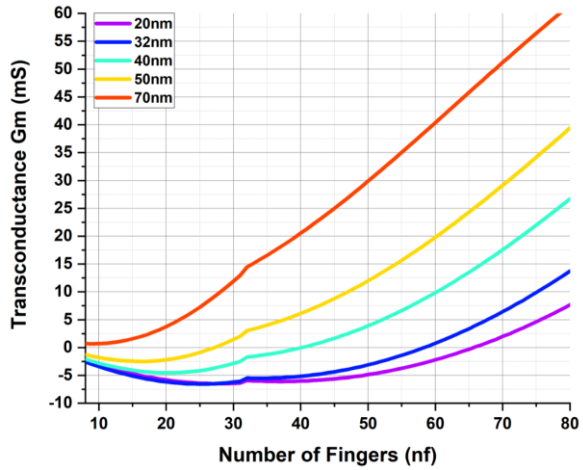
(b) Number of fingers vs. capacitance



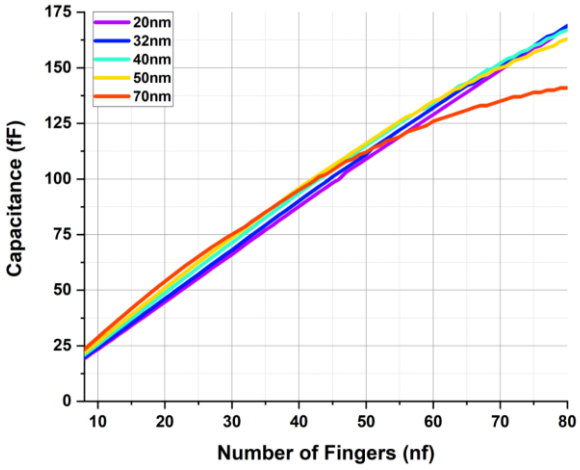
(c) Number of fingers vs. negative resistance

Figure 32. transconductance, capacitance and negative resistance at different relative finger widths (3x to 10x)

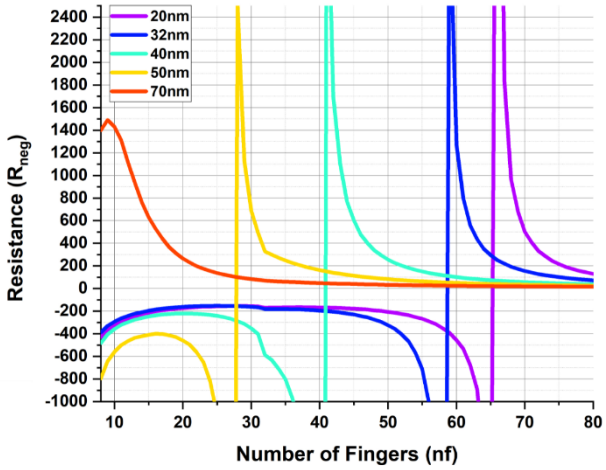
Figure 33 represents the second set of simulations that compare different parameters at different channel lengths, i.e., 20, 32, 40, 50, and 70 nm, respectively. The finger width was kept constant at 7x as selected from the previous set of simulations. From Figure 32(a), it can be illustrated that the 20 nm transistor achieves the maximum G_m, lowest capacitance C_{par} as compared to other transistors with higher channel length that contributes to an increase in the area of the device leading to higher capacitance and lower G_m.



(a) Number of fingers vs. transconductance G_m



(b) Number of fingers vs. capacitance



(c) Number of fingers vs. negative resistance

Figure 33. transconductance, capacitance and negative resistance at different channel lengths (20nm to 70nm)

3.3 Analysis and Design of LC Tank VCO

3.3.1 Design Flow

To summarize the guidelines mentioned earlier. The design flow of the oscillator will follow the below-mentioned methodology.

I. Select inductor (L) and varactor (C_{var}) for a required frequency of oscillation (F_{osc}). The oscillation frequency is calculated by

$$F_{osc} = \frac{1}{2\pi\sqrt{LC_{var}}} \tag{37}$$

II. Find the equivalent parallel losses R_P of the LC tank.
III. Determine the parasitic capacitance (C_{par}) of the CCP G_m stage as per negative resistance (R_{neg}). The oscillation frequency is then modified, taking into account the parasitic capacitance and is then expressed as:

$$F'_{osc} = \frac{1}{2\pi\sqrt{L(C_{var} + C_{par})}} \tag{38}$$

IV. Adjust inductor or varactor value to shift the oscillation frequency (F_{osc})
V. Finally, consider the buffer capacitance or other blocks loading the VCO to specify the tuning range, since the signal will be taken out differentially in this case. Therefore, twice the capacitance of the buffer will be taken into account.

3.3.2 Design Prototype 1: Conventional LC Tank VCO

Parametric Simulation of the LC Tank

LC tank is designed by connecting the inductor (L) and varactor (C_{var}) in the circuitry, as shown in the Figure 34, the input signal is provided differentially to calculate the output impedance of the circuitry. The impedance where it peaks is the parallel equivalent resistance (R_P). To begin with, a set of schematic simulations, the varactor, and the inductor were selected randomly so they can produce an oscillation frequency of approximately 100 GHz as a starting point. Then we can scale up things to reach a higher frequency.

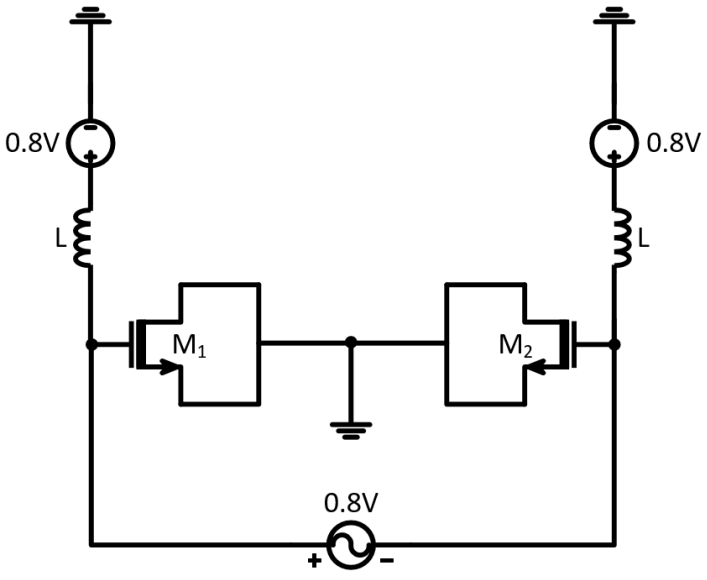


Figure 34. Simulation setup for LC Tank R_P Extraction

The first trial of dimensions of the Inductor (L) and varactor (C_{var}) are mentioned in Table 4 and Table 5.

Table 4. Spiral Inductor dimensions

Library Component	Inner Diameter (µm)	Turn width (µm)	No. of turns	Turn spacing (µm)	Inductance (pH)
Spiral Inductor (L)	34.2	4.5	**1**	4	100

Table 5. Library varactor dimensions

Library Component	Channel Length (nm)	Number of Fingers	Capacitance (fF)
Library Varactor (C_{var})	100	15	26.13

If we calculate the oscillation frequency considering the current data, it comes out to be

$$F_{osc} = \frac{1}{2\pi\sqrt{LC_{var}}} = 98.4\ GHz \tag{39}$$

Figure 35 illustrates the impedance vs. frequency plot of the LC tank. As seen from the Figure 35, the calculated frequency coincides with the simulation results. The LC tank has a parallel resonance frequency at 99.66 GHz and an equivalent parallel resistance (R_P) of 158.73 Ω.

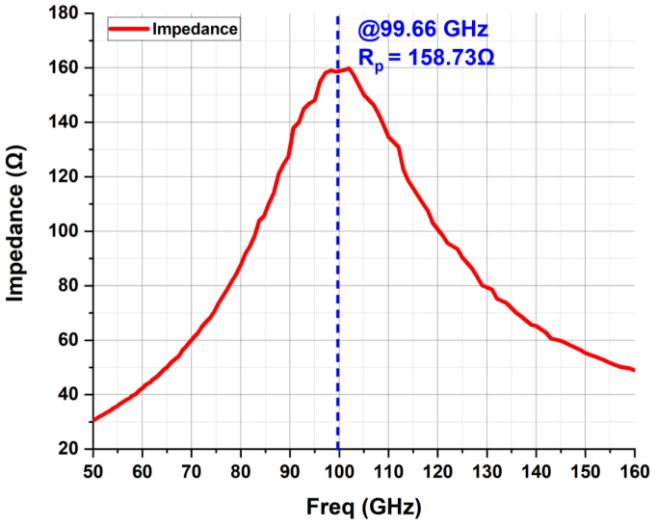


Figure 35. LC tank R_P Extraction without C_{par}

It is worth remembering that the G_m CCP stage parasitics are not considered yet in the oscillation frequency calculations. Those will be considered in the next section.

Parametric Simulation of the Negative Gm CCP stage

As discussed earlier, to satisfy the small-signal oscillation condition, the effective negative resistance $|R_{neg}|$ shall be smaller than $|R_P|$. Since at these frequencies, the calculations are only approximations. Taking G_m CCP parasitic capacitance into account the oscillation frequency and the start-up condition are given by

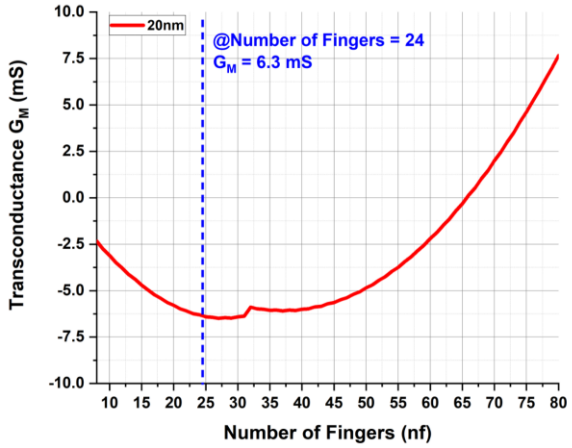
$$F'_{osc} = \frac{1}{2\pi\sqrt{L(C_{var} + C_{par})}} \tag{40}$$

$$G_m = \frac{g_m}{2} \geq \frac{1}{R_p} \tag{41}$$

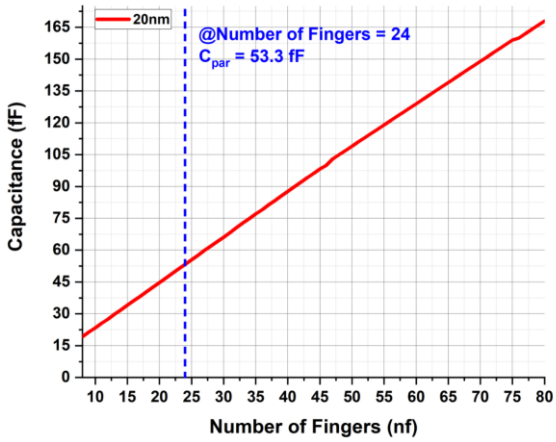
Figure 36 shows the transconductance, capacitance, and equivalent negative resistance produced by the CCP G_m stage. The CCP generates a transconductance of -6.3 mS, the parasitic capacitance of 53.3 fF and negative resistance of -158.7 Ω using 24 fingers. The size was selected after several iterations where the oscillation began and sustained. The dimensions of the G_m stage are given in Table 6.

Table 6. CCP G_M Stage dimensions

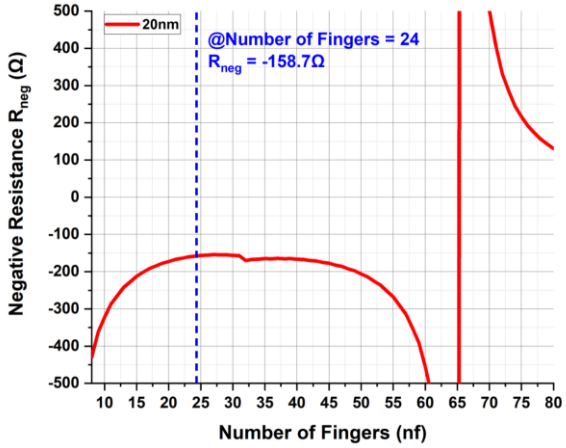
Component	Channel Length (nm)	Number of Fingers	G_M (mS)	C_{par} (fF)	R_{neg} (Ω)
CCP G_m Stage	20	24	-6.3	53.3	-159



(a) Number of fingers vs. transconductance G_M



(b) Number of fingers vs. capacitance C_{par}



(c) Number of fingers vs. negative resistance R_{neg}

Figure 36. transconductance, capacitance and negative resistance at finger width of 7x and channel length of 20nm

Considering the capacitance in the calculation of the oscillation frequency (F'_{osc}), the frequency will go down significantly as

$$F'_{osc} = \frac{1}{2\pi\sqrt{L(C_{var} + C_{par})}} = \frac{1}{2\pi\sqrt{100pH.(26.13fF + 53.3fF)}} = 56.4\ GHz \tag{42}$$

With the contribution of the parasitic capacitance (C_{par}) in the LC tank, the equivalent parallel resonance frequency changes. Also, the equivalent parallel resistance (R_P) is almost doubled, which can be seen in Figure 37.

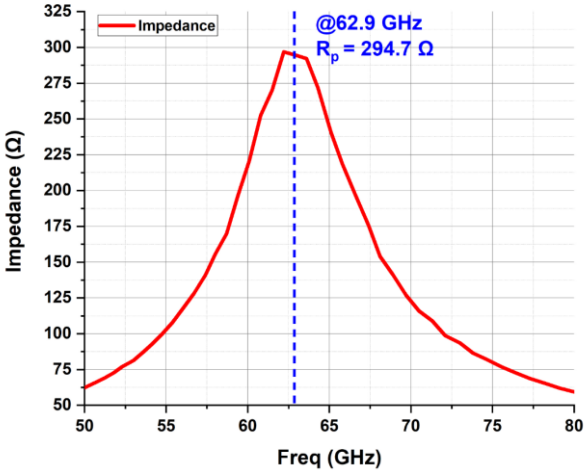


Figure 37. LC Tank Rp Extraction with C_{par}

PSS Simulation of the Oscillator Core

Previously discussed parameters of the oscillator core are summarized in Table 7 and satisfying the oscillation criteria mentioned in equation (41). The individual components are combined in the circuitry, as shown in Figure 38. Periodic steady-state (PSS) and phase noise simulations are performed, the circuit begins to oscillate at 63.48 GHz. The difference to the analyzed frequency is only 11%, indicating reasonable accuracy.

Table 7. Oscillator core parameters

Setup	L (pF)	C_{var} (fF)	C_{par} (fF)	R_P (Ω)	R_{neg} (Ω)	F'_{osc} Calculated (GHz)
Oscillator Core	100	26.13	53.3	294.7 Ω	-158.3	56.4

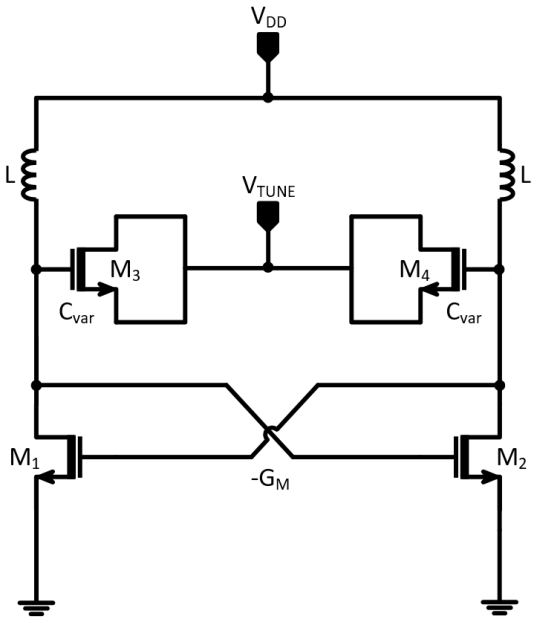
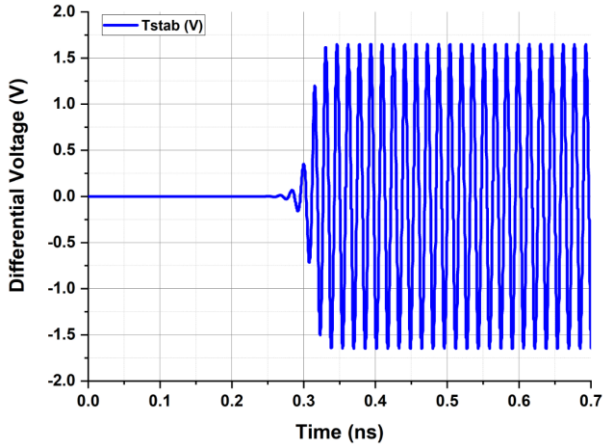


Figure 38. Oscillator Core Design

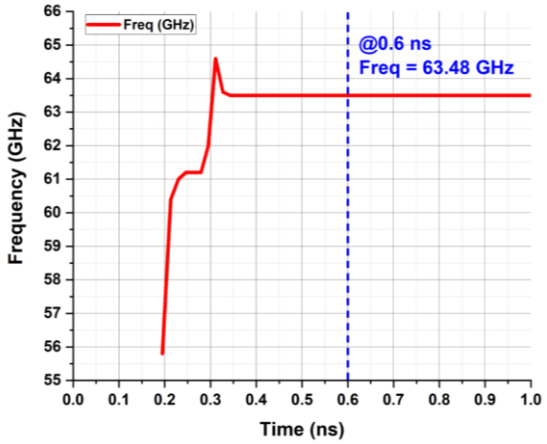
Table 8 shows detailed results of the oscillator core at 63.48 GHz, at V_{TUNE} of 0V with a phase noise of -110.4 dBc/Hz and output power of 11.13 dBm. The circuit was biased at 0.8V with a current I_d of 26.2 mA resulting in 21 mW power consumption.

Table 8. Oscillator core Trial-1 results

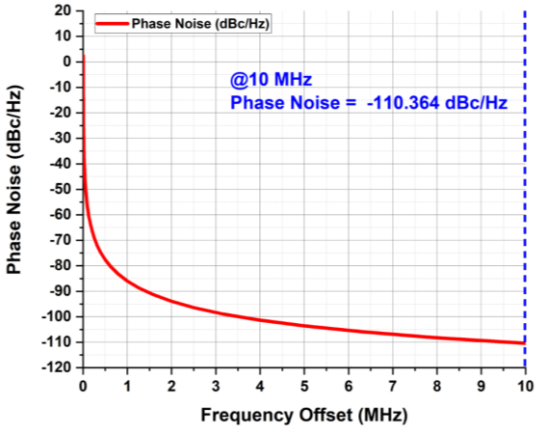
Oscillator Core	F'_{osc} - Simulated (GHz)	Phase Noise (dBc/Hz) @ 10MHz	Output Power (dBm)	Signal Swing (Vp-p)	V_{tune} (V)	V_{DD} (V)	I_d (mA)	P (mW)
Trial 1	63.48	-110.4	11.2	1.74	0	0.8	26.2	21



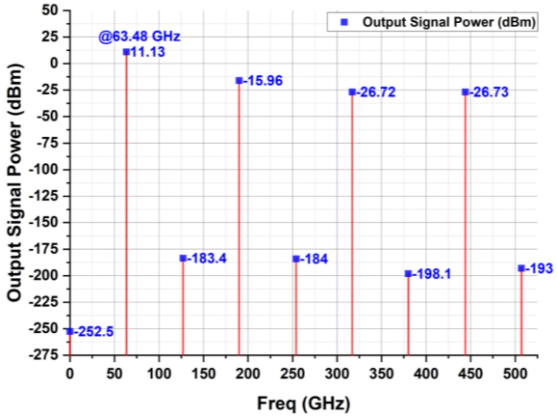
(a) Differential voltage (V)



(b) Oscillation frequency (GHz)



(c) Phase noise frequency offset (dBc/Hz)



(d) Output power at different harmonics (dBm)

Figure 39. Oscillator core Trial-1 results

To reach higher frequencies several different optimization strategies have been applied. Table 9 will demonstrate detailed results of the different practices adopted:

- **Trial 2: Reducing the size of the Inductor (L):** The self-resonance frequency of the inductor (L) shall be higher than the targeted oscillation frequency. Another thing to note is that reducing the size of the inductor will decrease parallel equivalent resistance R_P resulting in the requirement of a higher G_m value to compensate it. Thus increasing the power consumption and the parasitic capacitance C_{par}. As seen in Table 9, the size of the inductor

was reduced from 100pH to 50pH, resulting in the reduction of R_P from 295 to 197, while maintaining the start-up condition of oscillation thereby increasing the oscillation frequency from 63.5 GHz to 83 GHz with a phase noise of -107 dBc/Hz at V_{TUNE} = 0V achieved tuning range was 9%.

- **Trial 3: Reducing the size of the Transistors in CCP G_m Stage:** Reduction in the G_m will result in the decline in the parasitic capacitance C_{par} with the benefit of low power consumption in the CCP G_m stage. The reduction in G_m will increase the $R_{neg,}$ thereby overcompensating the R_P. Still, it begins to oscillate at a high frequency of 95 GHz with a phase noise of -104.3 dBc/Hz at V_{TUNE} = 0V and offers a high tuning range of 14%.
- **Trial 4: Reducing the size of the varactor (C_{var}):** The major drawback of reducing the size of the varactor is the reduction in the tuning range of the oscillator. This can be seen from Table 9 Trial 4 column having a Frequency Tuning Range (FTR) of 8%, with the benefit of higher oscillating frequency at 107 GHz having a phase noise of -101 dBc/Hz at V_{TUNE} =0V.

Table 9. Performance comparisons of different sets of LC tank implemented

Parameters	V_{TUNE} (V)	Trial 2	Trial 3	Trial 4
		Reducing the size of Inductor (L)	Reducing the size of the Transistors in CCP G_m Stage	Reducing the size of the varactor (C_{var})
L (pF)	**Nil**	**50**	50	50
C_{var} (fF)		26.1	26.1	**12.2**
C_{par} (fF)		53.3	34.0	34
R_P (Ω)		197	167.1	254
R_{neg} (Ω)		-158.3	-213	-213
F'_{osc} - Calculated (GHz)		80	92	105
F'_{osc} - Simulated (GHz)	**0**	83.1	95	107
Phase Noise (dBc/Hz) @ 10MHz	**0**	-107	-104.3	-101
Output Power (dBm)	**0**	9.51	6.74	8
Signal Swing (Vp-p)	**0**	1.3	1	1
Lower Freq (GHz)	**0**	83.1	95	107
Upper Freq (GHz)	**0.8**	91	109.1	115.1
FTR (%)	**0 to 0.8**	9	14.3	7.3
V_{DD} (V)	**0**	0.8	0.8	0.8
I(mA)	**0**	27	17	26.3
P(mW)	**0**	21.1	13.3	21
FOM_T		**-183**	**-187**	**-178**

As the comparison table demonstrates proper dimensioning leads to a high-frequency performance from the oscillators. To further go higher, the next sections will illustrate the optimization techniques employed to take it further.

Inductor Optimization

The inductor utilized in the previous design sets were library components. They were two single turn inductors each of 50 pH therefore making a total of 100 pH that is center-tapped to $V_{DD,}$ as seen from Figure 40 below.

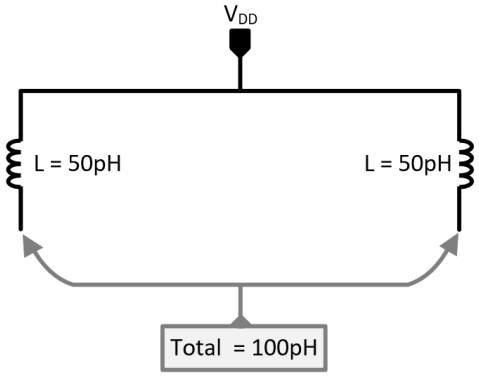
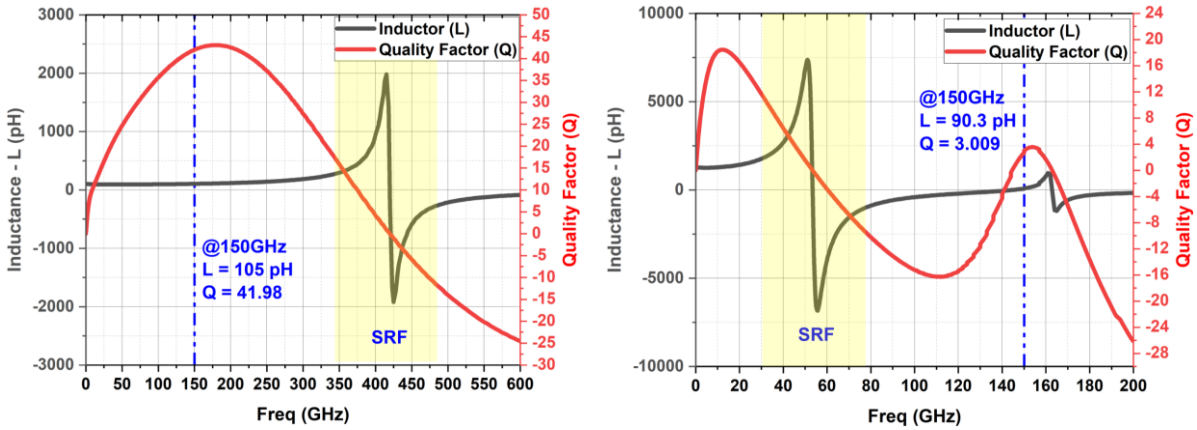


Figure 40. Inductance of LC Tank

The 100 pH (50+50) inductance had a self-resonance frequency (SRF) higher than the frequency of interest as illustrated in Figure 41(a) therefore they were utilized in the previous design iterations. To achieve a higher frequency of oscillation, the inductance shall be reduced further. Reducing the size of the inductance, from 100 pH to 90 pH, lowers the SRF as demonstrated in Figure 41(b) to be around 50 GHz. The SRF has distorted the quality factor due to its capacitive behavior at higher frequencies resulting in a lower quality factor of 3.009 at 150 GHz with an Inductance of 90.3 pH. This lead to the designing of the custom inductor.



(a) Inductance and quality factor (100 pH) (b) Inductance and quality factor (90 pH)

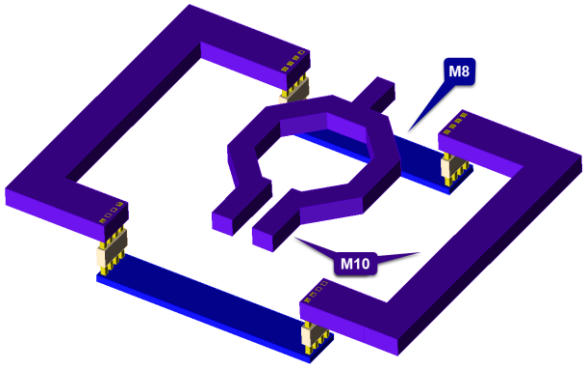
Figure 41. Inductance vs. quality factor plot at different inductor sizes

Symmetrical inductors characterized in Section 3.2.1 earlier can be scaled down to the required inductance value without compromising the quality factor of the inductor while keeping the SRF of the inductor higher than the oscillation frequency. The inductor and the ground planes were designed on an M10 layer. M8 layer was utilized to create an underpass on the ground planes to make a ground loop. The turn width of the inductor was kept at 6 µm, whereas the Inner diameter and the distance of the ground planes from the sides was kept at 27.93 µm. Table 10 represents the center-tapped symmetric inductor parameters.

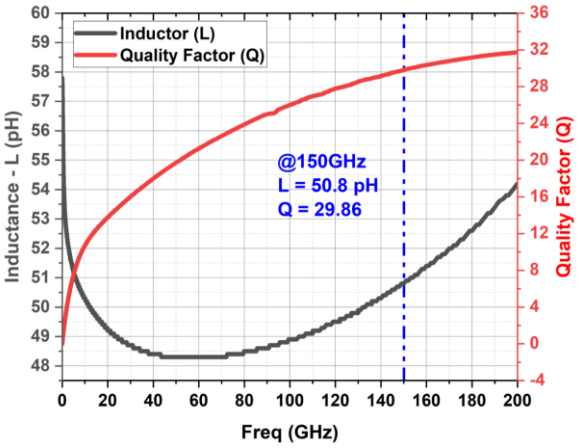
Table 10. Center-tapped symmetric inductor parameters

EM Component	No. of Turns	Inner diameter (µm)	Turn width (µm)	Space to side gnd planes (µm)	Inductance L (pH)	Total Inductance L+L (pH)	Q Factor
Center tapped symmetric inductor	1	28	6	28	25pH	50pH	30

Figure 42 demonstrates the drawn layout of the inductor in 3D as seen in Figure 42 (a). The inductor has a total Inductance of 50 pH with a quality factor of 29.86, as illustrated in Figure 42(b).



(a) 3D Layout view



(c) Inductance and quality factor (EM simulated design results)

Figure 42. 50 pH (25+25) Inductor design

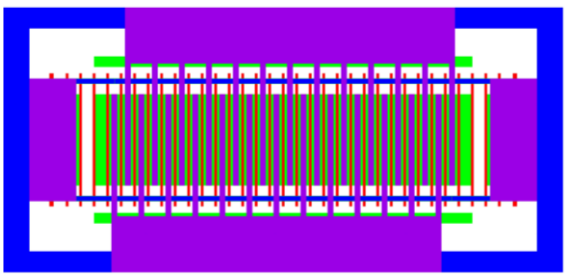
The reduction in the size of the inductor will produce a low R_P. To compensate it, the size of the transistor in G_m CCP pair is increased to generate more transconductance (G_m), i.e., less R_{neg} to cancel the losses produced by the tank. With the reduction of Inductor (L) from 50pH to 25pH, the G_m transistor size was redimensioned with added width by 50%. It began oscillating at 126 GHz with a phase noise of -102 dBc/Hz and a frequency tuning range of 6%. Table 11 demonstrates the detailed parameters and results obtained with the design.

Table 11. Inductor (L) scaling and VCO optimization

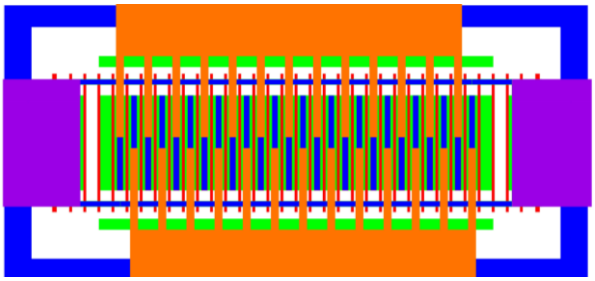
Parameters	**V_{TUNE} (V)**	**Trial 5**
		Inductor (L) scaling and optimization
L (pF)	**Nil**	**25**
C_{var} (fF)		12.3
C_{par} (fF)		56
R_P (Ω)		165
R_{neg} (Ω)		-157
F'_{osc} - Calculated (GHz)		122.2
F'_{osc} - Simulated (GHz)	**0**	126
Phase Noise (dBc/Hz) @ 10MHz	**0**	-102
Output Power (dBm)	**0**	6
Signal Swing (Vp-p)	**0**	0.8
Lower Freq (GHz)	**0**	126
Upper Freq (GHz)	**0.8**	133.4
FTR (%)	**0 to 0.8**	6
V_{DD} (V)	**0**	0.8
I(mA)	**0**	28
P(mW)	**0**	22
FOM_T		**-178**

G_M CCP Transistors Layout Optimization

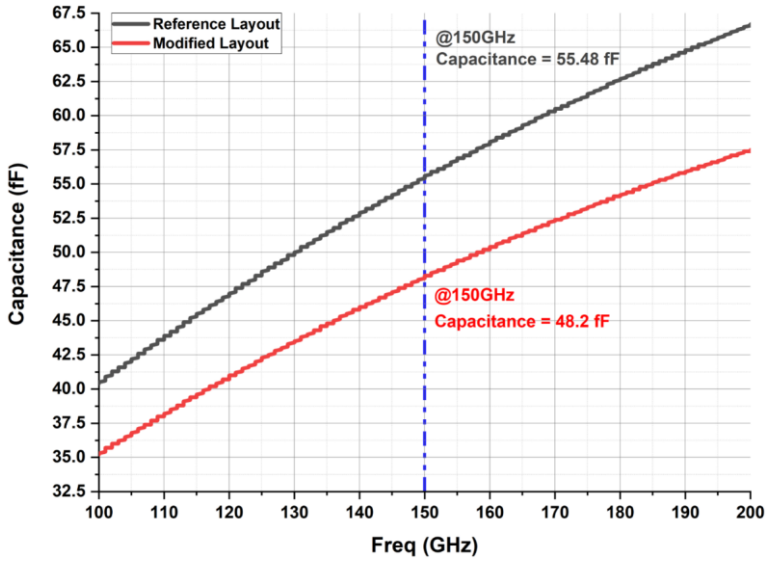
The layout of the transistors at CCP G_m stage can be optimized by making the traces to be half strapped taken from drain to source thus benefiting with the reduction in the parasitic capacitances especially C_{DS} (capacitance from drain to source) also experiencing a decline in the gate to source (C_{GS}) and gate to drain (C_{GD}) capacitances as well. The reduction in parasitics was observed to be 7.18fF which can be seen from Figure 43(a) and (b) where the modification in the layout can be visibly seen.



(a) Reference Transistor Layout
(Full-strapped Drain and Gate)



(b) Modified Transistor Layout
(Half-strapped Drain and Gate)



(c) Comparison of capacitances of the reference and the improved layouts

Figure 43. CCP G_m transistor layout design and capacitance comparison

Due to reduction in the parasitics from 55fF to 48.3fF, the oscillation frequency was increased from 126 to 132.2 GHz with a phase noise of -100 at V_{TUNE} = 0 and a frequency tuning range of 7% which can be seen from the Trial 6 of the design in Table 12.

Table 12. G_m Stage transistor layout optimization parameters and VCO simulation results

Parameters	V_{TUNE} (V)	Trial 6
		G_M Stage Transistor Layout Optimization
L (pF)	**Nil**	25
C_{var} (fF)		12.3
C_{par} (fF)		**48.2**
R_P (Ω)		165
R_{neg} (Ω)		-140
F'_{osc} - Calculated (GHz)		122.2
F'_{osc} - Simulated (GHz)	**0**	132.2
Phase Noise (dBc/Hz) @ 10MHz	**0**	-100
Output Power (dBm)	**0**	4.7
Signal Swing (Vp-p)	**0**	1
Lower Freq (GHz)	**0**	132.2
Upper Freq (GHz)	**0.8**	142
FTR (%)	**0 to 0.8**	7
V_{DD} (V)	**0**	0.8
I(mA)	**0**	27
P(mW)	**0**	21.2
FOM_T		**-178**

Final Design Implementation

The previous design iterations have shown the oscillation frequency sensitivity towards its parasitics. After multiple trials to optimize the oscillation frequency, further trials to target higher frequency by reducing the size of the inductor don't satisfy the oscillation criteria and the oscillation dies away. The dimensions of the inductor and the transistors discussed in the previous section are the final ones. These are taken forward for the final implementation. A layout was constructed including the top-level metallic layers to take into account further parasitic effects.

As a starting point, the layout of the transistors in the G_m CCP stage and the varactor are at low metallic layers (M1-M5). Thus, taking up to higher metallic layers will add further parasitics, reducing the oscillation frequency. This section will focus on the impacts of parasitics on the performance parameters discussed earlier. The varactor and the G_m transistors were taken to the M7 level. The parasitic extraction (PEX) was performed. The G_m stage and varactor were connected with vias to the inductor.

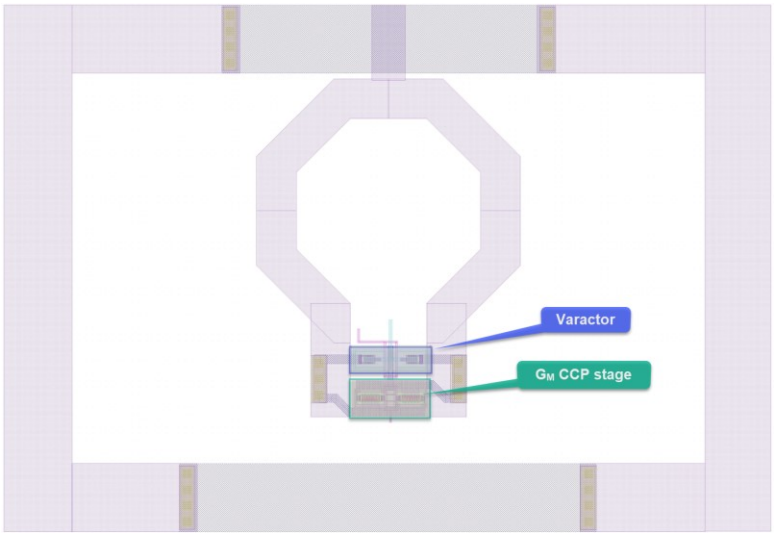


Figure 44. Oscillator core design prototype 1

The additional parasitic capacitance contributed by the extra metallic layers and the parasitic inductance introduced by the vias has resulted in the reduction of 3.2 GHz in frequency from 132.2 GHz to 129 GHz with a phase noise of -101.2 dBc/Hz having a high output power of 4.2 dBm as illustrated in Table 13. The oscillator has a decent tuning range of 6.4%. The circuit is rather power-hungry and consumes DC power of 21.3 mW. The next section will look into another technique to reduce the DC power consumed by the oscillator.

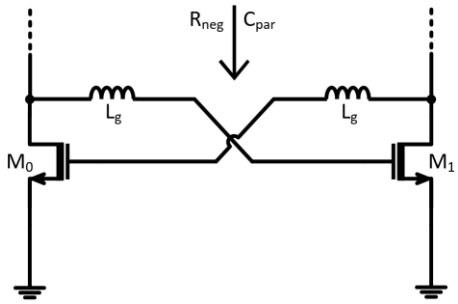
Table 13. Performance parameters of design prototype 1

Parameters	**V_{TUNE} (V)**	**Final design update**
		Varactor and G_m Stage (M1-M7 Layer)
F'_{osc} - Simulated (GHz)	**0**	129
Phase Noise (dBc/Hz) @ 10MHz	**0**	-101.2
Output Power (dBm)	**0**	4.2
Signal Swing (Vp-p)	**0**	1
Lower Freq (GHz)	**0**	129
Upper Freq (GHz)	**0.8**	137.1
FTR (%)	**0 to 0.8**	6.4
V_{DD} (V)	**0**	0.8
I(mA)	**0**	27
P(mW)	**0**	21.3
FOM_T		**-176**

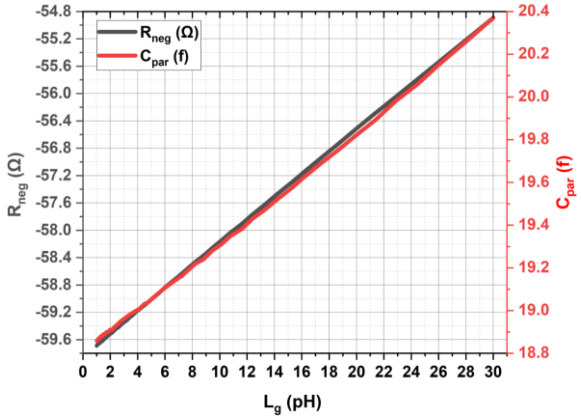
3.3.3 Design Prototype 2: LC Tank VCO with Inductive divider CCP

As observed in the previous oscillator core designs, the circuitry consumes a high DC power. The largest part comes from the G_m CCP stage. A technique to reduce this power is to reduce the size of the G_m CCP transistors by utilizing an inductive divider L_g as shown in the schematic diagram in Figure 45(a). The ideal inductors L_g act as an inductive divider with impedance boosting characteristics [35]. Using the inductive divider, L_g assists in increasing the negative resistance, as depicted in Figure 45(b), (c), and (d). Consequently, the size of the G_m CCP transistor size is reduced, thus decreasing the fixed capacitance of G_m, thereby theoretically assist in an increase in tuning range [9]. The technique has been effectively implemented at 64

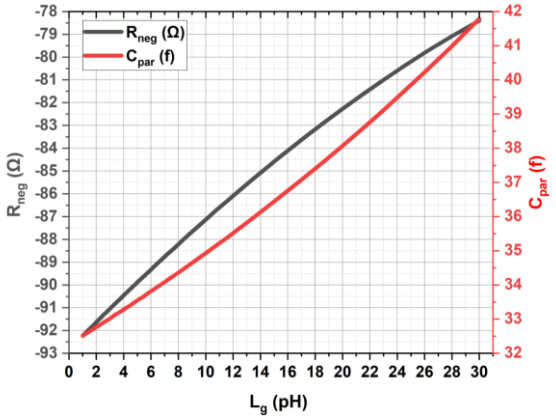
GHz and 118 GHz [35] and [9], respectively. It is important to realize the limitation of this technique, which is being demonstrated in the figures below.



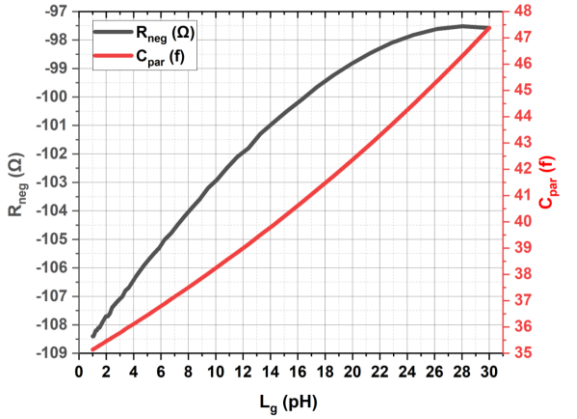
(a) Schematic of the Inductive divider in the CCP



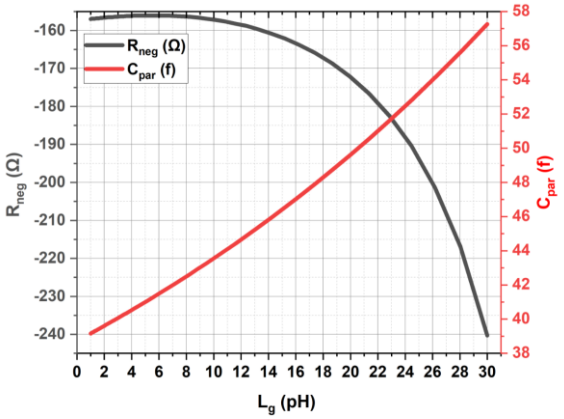
(b) At 65 GHz (R_{neg} and C_{par} versus L_g)



(c) At 118 GHz (R_{neg} and C_{par} versus L_g)



(d) At 130 GHz (R_{neg} and C_{par} versus L_g)



(e) At 150 GHz (R_{neg} and C_{par} versus L_g)

Figure 45.The negative resistance R_{neg} and the parasitic capacitance C_{par} of the CCP versus the inductance L_g

As shown in Figure 45(b), (c) and (d), which are plotted at 65, 118, and 130 GHz showed an increase in the negative resistance by 13%, 14%, and 9.2%, respectively. Whereas, after 130 GHz, i.e., at 150 GHz, the negative resistance tends to decrease by 50%, as shown in Figure 45 (e). The behaviour can be explained from the plot in Figure 46, which illustrates the negative resistance (R_{neg}) at different Inductance (L_g) values. As seen from the graphical representation, the R_{neg} of the G_m CCP steadily begin to decrease, starting from 138 GHz as it begins to approach its self-resonance frequency. With the increase in L_g value, the SRF approaches quickly, thus demonstrating a decrease in R_{neg} with an increase in the inductance value (L_g) as depicted in Figure 45(e).

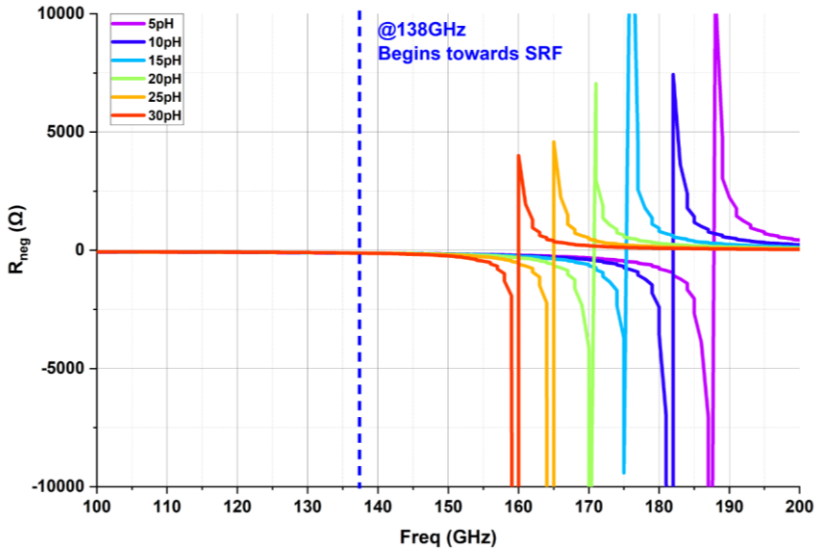
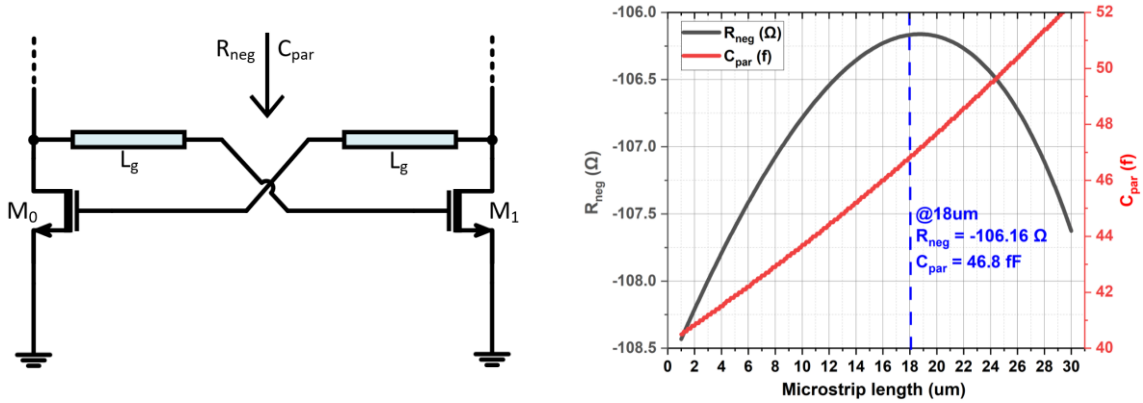


Figure 46. R_{neg} vs. frequency plot at a different value of inductance values (L_g)

Since currently, the oscillation frequency is less than 150 GHz and is oscillating at 130 GHz, as observed in the previous section results, we can implement this technique by considering the Figure 45(c). As seen from the figure, the ideal inductance required is low around 25 pH, which will increase the negative resistance from -108 Ω to -98 Ω i.e., about 9.2%. This low inductance can be implemented by utilizing a transmission line, which is a distributed element of RLGC (resistance, inductance, conductance and capacitance) whose line length can be found by the simulation in Figure 47. The transmission line as an inductor implementation has given the increase in negative resistance from -108.5 Ω to -106.7 Ω, which is quite low, i.e., 1.8% seen from the Figure 47(b) as compared to the ideal inductor. For this section, the transmission line as an inductor is selected to be employed in the inductive divider CCP oscillator. It is to be noted that all the simulations were carried out with constant transistor size in the CCP, which was selected after multiple iterations. These dimensions are taken forward for the oscillator design.

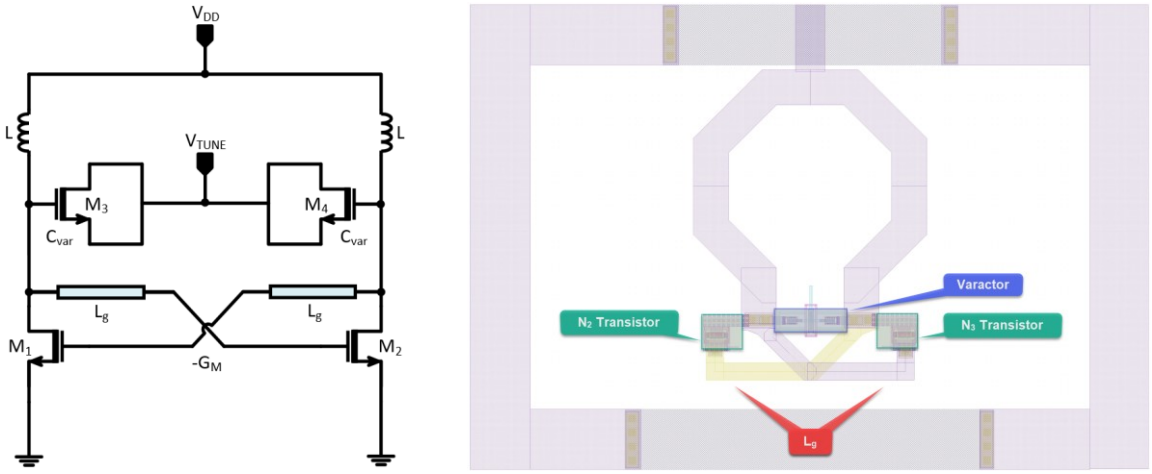


(a) Schematic of the transmission line as an inductive divider

(b) At 130 GHz (R_{neg} and C_{par} versus Transmission line length (μm))

Figure 47. The negative resistance R_{neg} and the parasitic capacitance C_{par} of the CCP versus the inductance L_g

Figure 48 demonstrates the schematic diagram and the layout design of the oscillator with inductive divider CCP. The dimensions of the CCP transistor were selected after multiple iterations until the negative resistance R_{neg} became large enough to cancel the losses of the LC tank. The LC tank dimensions were chosen to be the same as the one described in the final design of Section 3.3.2.



(a) Schematic diagram (b) Layout

Figure 48. Schematic and layout of the oscillator core design prototype 2

The Table 14 demonstrates the simulation results of the oscillator core shown in Figure 48. The oscillator oscillates at 126.2 GHz which was close to the calculated value, with a phase noise of -102.5 dBc/Hz at V_{TUNE} voltage of 0V with a signal output power of 3.6 dBm. It has a tuning range of 5.4% from 126.2 to 133.2 GHz. The transistor consumes a DC power of 17.1 mW, which is better than previous designs, but if we compare it to the state-of-the-art designs it is still high. Moving forward, the next section will look at the detailed comparison of the two design methodologies discussed. Further solutions will be discussed to design the oscillator core more power efficient.

Table 14. Oscillator core design prototype 02 parameters and simulation results

Parameters	**V_{TUNE} (V)**	**Final design update**
		Inductive divider in CCP
L (pF)	**Nil**	25
C_{var} (fF)		12.3
C_{par} (fF)		51
R_P (Ω)		160
R_{neg} (Ω)		-178
F'_{osc} - Calculated (GHz)		127
F'_{osc} - Simulated (GHz)	**0**	126.2
Phase Noise (dBc/Hz) @ 10MHz	**0**	-103.5
Output Power (dBm)	**0**	3.6
Signal Swing (Vp-p)	**0**	0.7
Lower Freq (GHz)	**0**	126.2
Upper Freq (GHz)	**0.8**	133.1
FTR (%)	**0 to 0.8**	5.4
V_{DD} (V)	**0**	0.8
I(mA)	**0**	21.4
P(mW)	**0**	17.1
FOM_T		**-178.2**

3.3.4 Comparison of the Two Designs

In order to compare the two oscillator designs in Sections 3.3.2 and 3.3.3, we will examine the performance of the two design methodologies with frequency pushing, which is described as the VCO sensitivity to the variation in the supply voltages. The performance limitation of the design will be observed with this trial. This will assist in choosing the supply voltage suitable to produce oscillations without the consumption of high DC current, although compromising some of the performance. Table 15 and Table 16 illustrate the performance of the two design methodologies.

Table 15. Performance of the Conventional LC Tank VCO with frequency pushing

Parameters	**V_{TUNE} (V)**	**Design Prototype 1: Conventional LC tank VCO**							
F'_{osc} - Simulated (GHz)	**0**	128.7	129	129.3	130.1	131.5	133.4	136.2	140
Phase Noise (dBc/Hz) @ 10MHz	**0**	-101.2	-102	-101.5	-101	-100.4	-99.3	-97.8	-95.9
Output Power (dBm)	**0**	4.2	4	4.1	3	3.5	3	2.3	1.3
Signal Swing (Vp-p)	**0**	0.9	0.9	0.9	0.8	0.7	0.6	0.5	0.4
Lower Freq (GHz)	**0**	128.7	129	129.3	130.1	131.5	133.4	136.2	140
Upper Freq (GHz)	**0.8**	137.1	137	137.1	138	139	140	141.81	144.2
FTR (%)	**0 to 0.8**	6.4	6	5.9	5.6	5.3	4.8	4	3
V_{DD} (V)	**0**	**0.8**	**0.75**	**0.7**	**0.65**	**0.6**	**0.55**	**0.5**	**0.45**
I(mA)	**0**	27	24	20.6	17.48	14.4	11.4	8.5	6
P(mW)	**0**	21.3	18	14.4	11.36	9	6.3	4.3	2.7
FOM_T		**-178.5**	**-178.5**	**-178.1**	**-177.5**	**-176.5**	**-175**	**-172.1**	**-168.1**

To compare performance between the two design methodologies presented in Table 15 and Table 16, the conventional CCP LC tank design is on par with the inductive divider CCP design. At $V_{TUNE} = 0$ and $V_{DD} = 0.8$ V, the conventional design prototype 1 oscillates at a frequency of 128.7 GHz with a phase noise of -101.2 dBc/Hz as compared to prototype 2, which oscillates at 126.22 GHz with a phase noise of -102.5 dBc / Hz. Slight improvement in phase noise is observed. If we compare the tuning of the two oscillator designs, the design prototype 1 performs better and has a higher tuning range of 6.4% as compared to the design prototype 2.

The frequency pushing has assisted in the reduction of the parasitic capacitance by drawing less current when varied from 0.8V to 0.45V, thus increasing the oscillation frequency. In contrast, a decrease in the overall FTR (frequency tuning range) observed for both the design methodologies. Reducing the V_{DD} further, i.e., 0.4V dampens the oscillation and the VCO doesn't achieve the steady-state. A reduction in output signal power can be seen, which is expected with the decrease in V_{DD} supply voltage. The DC power consumed is less with V_{DD} variation, with some compromises in the performance parameters. If the current can be controlled through the oscillator core, we can benefit from decent power consumption from the core with satisfactory performance. This can be achieved with the current mirror on top of the oscillator core that controls the current passing through the core.

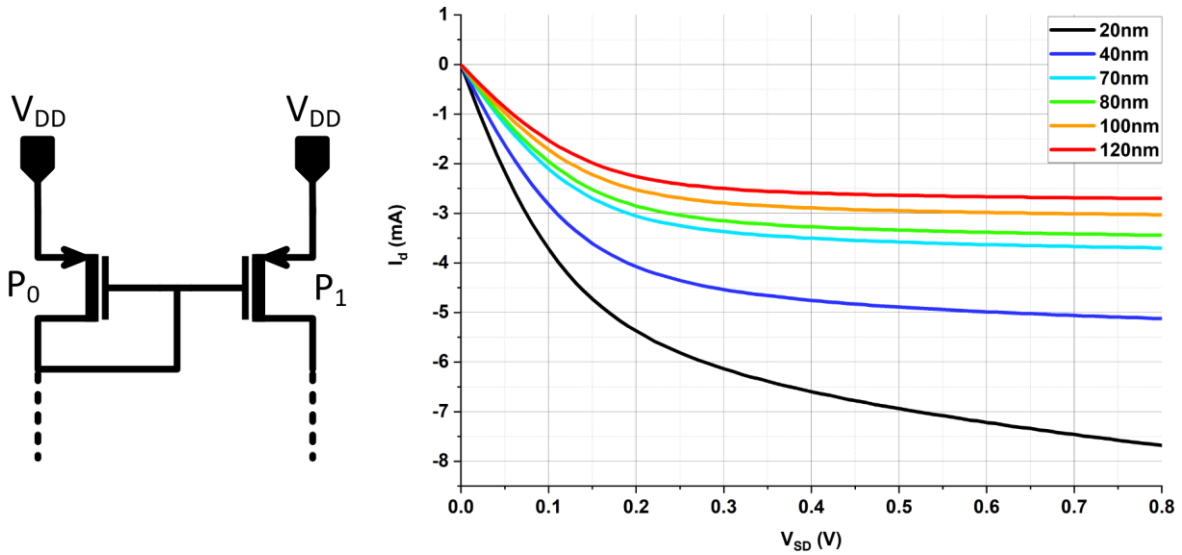
It is clear from the tables presented that design prototype 1 performs better and shall be taken forward to the next design phase. As seen from Table 15, V_{DD} of 0.6V seems to be an excellent choice oscillating at 131.5 GHz with a phase noise of -100.4 dBc/Hz. In terms of the tuning range, there is a reduction of 1.1% from 6.3% to 5.3% when transitioning from 0.8V to 0.6V. The total supply voltage required will be 1.2 V divided across the current mirror and G_m CCP stage.

Table 16. Performance of the LC Tank VCO with inductive divider CCP utilizing frequency pushing

Parameters	**V_{TUNE} (V)**	**Design Prototype 2: LC tank VCO with inductive divider CCP**							
F'_{osc} - Simulated (GHz)	**0**	126.2	126.4	127	127.5	128.5	130.1	132.3	135.3
Phase Noise (dBc/Hz) @ 10MHz	**0**	-102.5	-103	-103	-102.5	-101.8	-101	-99.4	-98
Output Power (dBm)	**0**	3.6	3.7	3.6	3.3	3	2.4	1.8	0.8
Signal Swing (Vp-p)	**0**	0.7	0.9	0.7	0.7	0.6	0.6	0.5	0.4
Lower Freq (GHz)	**0**	126.2	126.4	127	127.4	128.5	130.1	132.3	135.3
Upper Freq (GHz)	**0.8**	133.2	132.9	133	133.4	134.2	135.3	136.7	138.6
FTR (%)	**0 to 0.8**	5.4	5	4.8	4.5	4.3	4	3.3	2.4
V_{DD} (V)	**0**	**0.8**	**0.75**	**0.7**	**0.65**	**0.6**	**0.55**	**0.50**	**0.45**
I(mA)	**0**	21.4	19	16.5	14	11.6	9.2	7	5
P(mW)	**0**	17.1	143	11.6	9.2	7	5	3.5	2.2
FOM_T		**-178**	**-178**	**-178**	**-177**	**-176**	**-174**	**-172**	**-168**

3.3.5 Current Mirror Implementation and Dimensioning

The current mirror will be implemented to control the VCO core current. Figure 49(a) shows the basic current mirror topology implemented with the PMOS transistors. Figure 49(b) illustrates the DC simulations of the PMOS current mirror of different transistor channel lengths with a constant width. These simulations enlighten the short channel effects and show that smaller channel length transistors are unsuitable for this kind of application. From the figure, it can be observed that a channel length of more than 70 nm is suitable to assume the behaviour of the current generator.



(a). Basic current mirror (b) DC simulation of the basic current mirror

Figure 49. Schematic and simulation of the PMOS current mirror

PFET transistors with a channel length of 80 nm were chosen to avoid short channel effects to have a stable 1:10 division current ratio between P_0 and P_1 transistors. The W/L ratio of the G_m CCP stage was 875, and the current mirror was selected to have a W/L ratio close to the G_m CCP stage to have a voltage division of 0.6V each, i.e., in the G_m CCP stage and the current mirror. The P_1 transistor was dimensioned by keeping the W/L ratio of 1000, whereas P_0 was ten times less than P_1.

The performance of the oscillator is observed after the implementation of the current mirror. There is not a significant change in the performance as compared to the previous iteration of results. The oscillator is oscillating at 131 GHz with a phase noise of -99 dBc/Hz at $V_{TUNE} = 0$ with a signal swing of 0.8 V_{p-p}. It has a decent figure of merit where the core power is consuming less power, i.e., around 9 mW. The oscillator core contains the G_m CCP stage and the LC tank biased at 0.6V whereas the oscillator circuit also includes the PMOS current in addition to the mentioned components earlier and is biased 1.2V. The oscillator depicts a decent tuning range of 5.24%.

Table 17. Performance parameters of design prototype 1 with PMOS current mirror

Parameters	**V_{TUNE} (V)**	**Design Prototype 01**	
		Current mirror implementation (1:10 ratio)	
F'_{osc} - Simulated (GHz)	**0**	131	
Phase Noise (dBc/Hz) @ 10MHz	**0**	-99	
Output Power (dBm)	**0**	3.7	
Signal Swing (Vp-p)	**0**	0.8	
Lower Freq (GHz)	**0**	131	
Upper Freq (GHz)	**0.8**	138	
FTR (%)	**0 to 0.8**	5.2	
Parameters	**V_{TUNE} (V)**	**Oscillator circuit with biasing**	**Oscillator Core**
V_{DD} (V)	**0**	1.2	0.6
I(mA)	**0**	17.4	15
P(mW)	**0**	21	9
FOM_T			**-175**

3.3.6 Buffer Design 1: Source Follower

This section will discuss the implementation of the buffer addressed earlier in Section 2.6.1. As discussed earlier, the idea to drive a low output impedance load of 50 Ω at the oscillator core for measurements. The source follower has a high input impedance and low output impedance. Thus, it inherently carries high current. Below procedure was adopted to design the buffer. First, the width of the transistors is determined. This is achieved by choosing the transistor size to have a g_m of 20 mS since it will define the real part of the impedance to be 50 Ω. The next step is to utilize the transmission line stubs to cancel the imaginary part, thus matching it to 50 Ω real impedance.

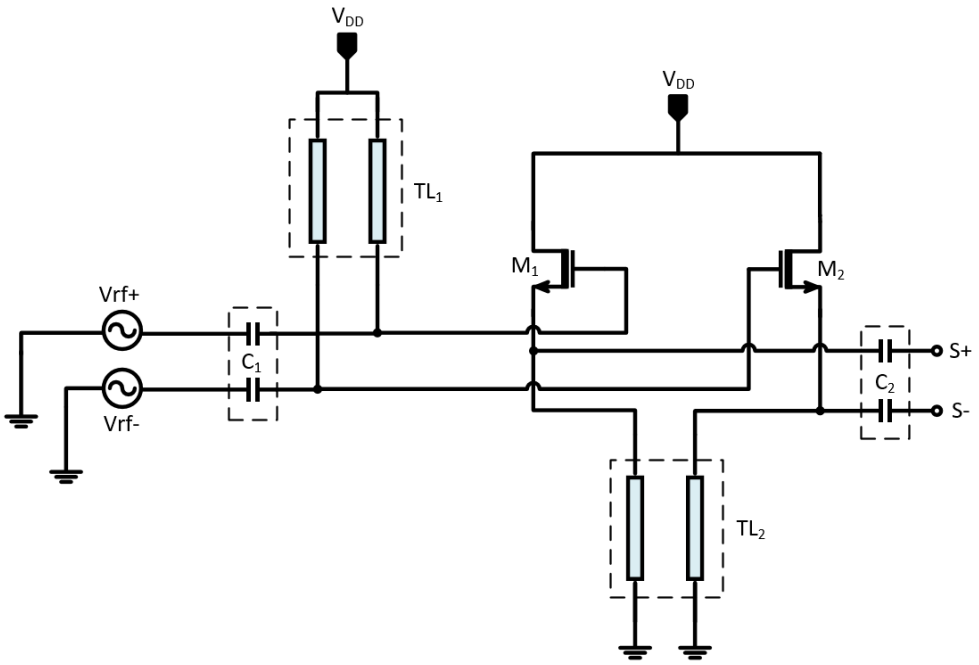
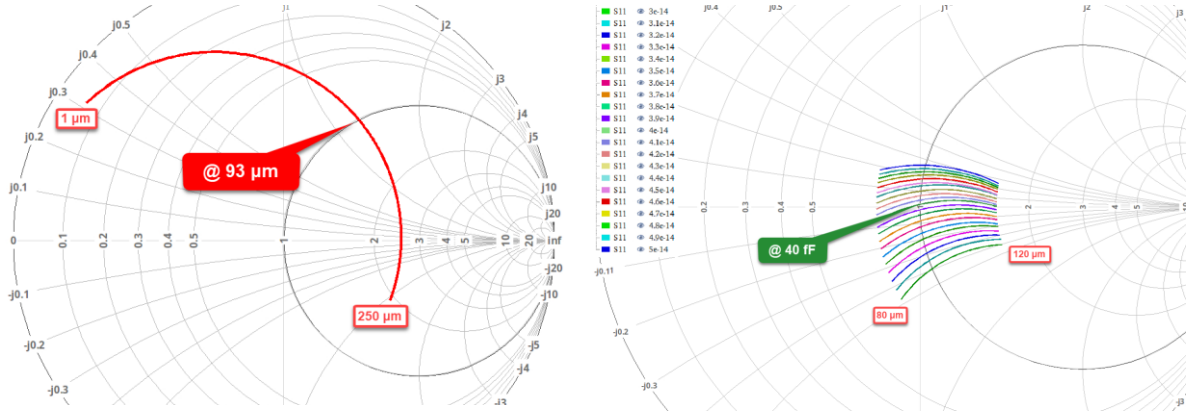


Figure 50. The source follower buffer circuit

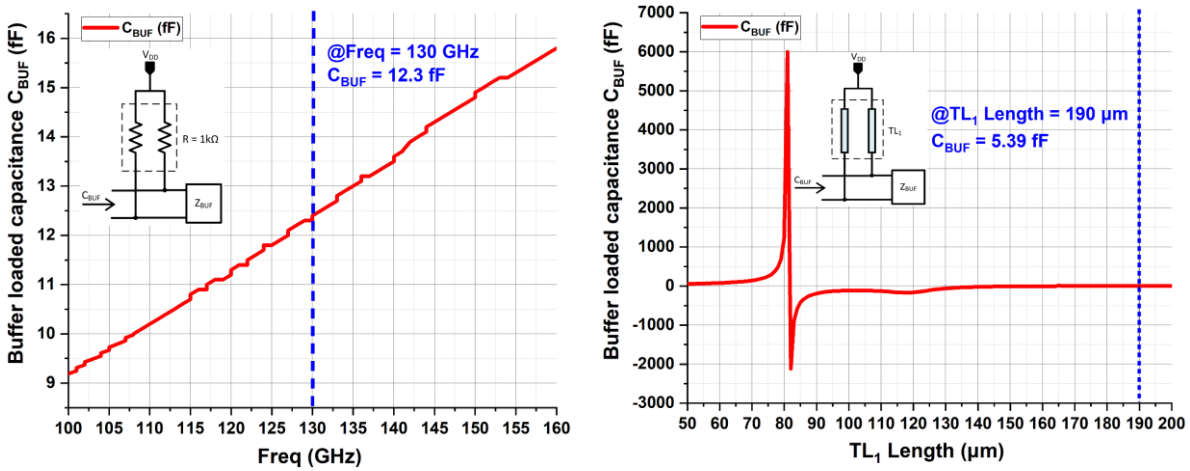
Figure 51 illustrates the matching procedure explained earlier after selecting the transistor width to have a g_m of 20 mS. The TL_2 was swept from 1μm to 250 μm. The arc formed will intersect the smith chart "unity" circle at 93 μm of transmission line length TL_2 as demonstrated in Figure 51(a). At this point of matching, C_2 was removed and TL_1 was replaced with a 1 kΩ of resistance connected to V_{DD}, allowing the signal to pass through the transistor. After choosing the length of the TL_2, the C_2 capacitor value was swept from 30 to 50 fF. The point where it intersects the center of the Smith chart is matched to 50 Ω, i.e., at 40 fF.



(a) TL_2 length swept from 1µm to 250µm (b) TL_2 swept from 80µm to 120µm at different C_2 values

Figure 51. TL_2 and C_2 values swept at 130 GHz

After the matching, if we tried to minimize the loaded capacitance parallel to high interstage biasing resistance of 1 kΩ connected to $V_{DD,}$ as seen in Figure 52(a). The loaded capacitance of the buffer is 12.3 fF. The resistance R can be replaced with an equivalent transmission line of λ/4, which will create a high impedance point at 130 GHz for the signal not leak into the supply (V_{DD}). Alternatively, we can optimize this transmission line length, thus lowering the loaded capacitance also fulfilling the requirement of a high impedance point as well. This is demonstrated in Figure 52(b). The transmission (TL_1) length was swept from 50 µm to 200 µm, and the loaded capacitance variation can be seen correspondingly. It is to be noted that the transmission line shall be chosen to be close to λ/4 in this scenario, it was selected to be 190 µm at which we are able to achieve a loaded capacitance of 5.39 fF.



(a) Loaded capacitance with R = 1kΩ (b) Loaded capacitance with TL_1

Figure 52. Optimization of the loaded capacitance of the buffer

Table 18. Design parameters of the source follower buffer circuit

C_1 (fF)	C_2 (fF)	TL_1 (um)	TL_2 (um)
30	40	93	190

Table 18 demonstrates the design parameters of the source follower buffer in Figure 50. The performance of the buffer circuit was verified, and Table 19 illustrates the performance parameters of the design. The oscillator oscillates at 124 GHz with a phase noise of

-100.3 dBc/Hz at V_{TUNE} = 0. The tuning range of the oscillator is 3.4%, with a variation in V_{TUNE} from 0 to 0.8V. The output signal power was -7.3 dBm at V_{TUNE} = 0. The oscillator core is consuming power of 9 mW, whereas the buffer core consumes a power of 13 mW.

Table 19. Performance parameters of the oscillator with source follower buffer circuit design

Parameters	V_{TUNE} (V)	Design Prototype 1
		Source follower buffer circuit
F'_{osc} - Simulated (GHz)	0	124
Phase Noise (dBc/Hz) @ 10MHz	0	-100.3
Output Power (dBm)	0	-7.3
Signal Swing (Vp-p)	0	0.24
Lower Freq (GHz)	0	124
Upper Freq (GHz)	0.8	128.1
FTR (%)	0 to 0.8	3.4

Parameters	V_{TUNE} (V)	Oscillator circuit with biasing	Oscillator Core	Buffer Circuit
V_{DD} (V)	0	1.2	0.6	0.8
I(mA)	0	16.4	15	16
P(mW)	0	20	9	13
FOM_T				-173

3.3.7 Buffer Design 2: Common source

The buffer addressed earlier in Section 2.6.2 will be discussed as an alternative approach in this section. Getting started with the buffer design, Figure 53 illustrates the buffer circuit, as demonstrated earlier. In contrast, the only difference is the M_3 and M_4 transistors act here as the feedback capacitors C_n performing the feedback tuning, i.e., capacitive neutralization, as explained earlier in Section 2.6.2.

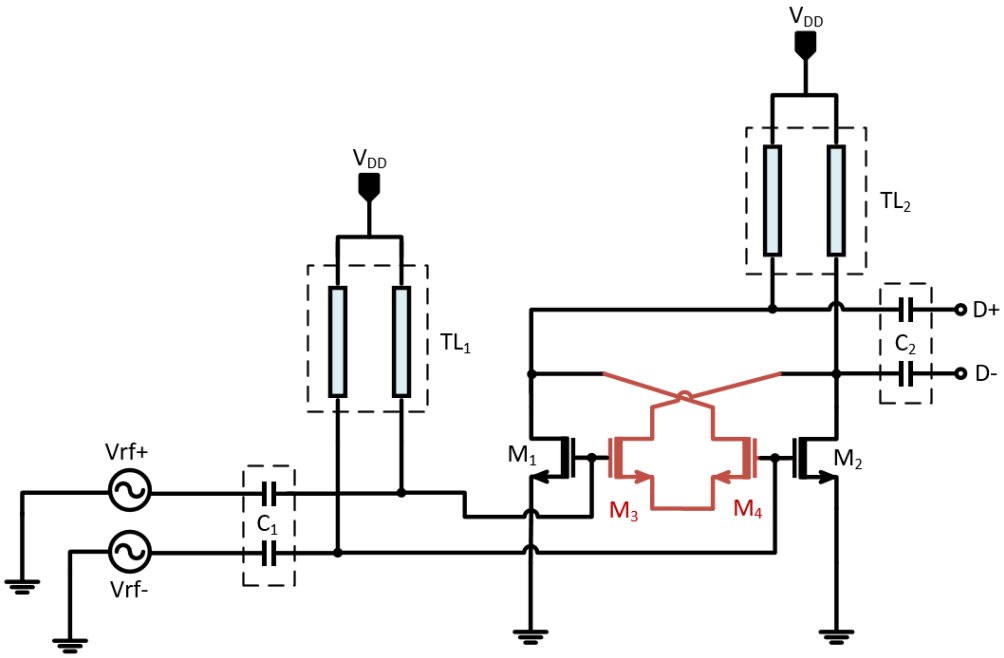
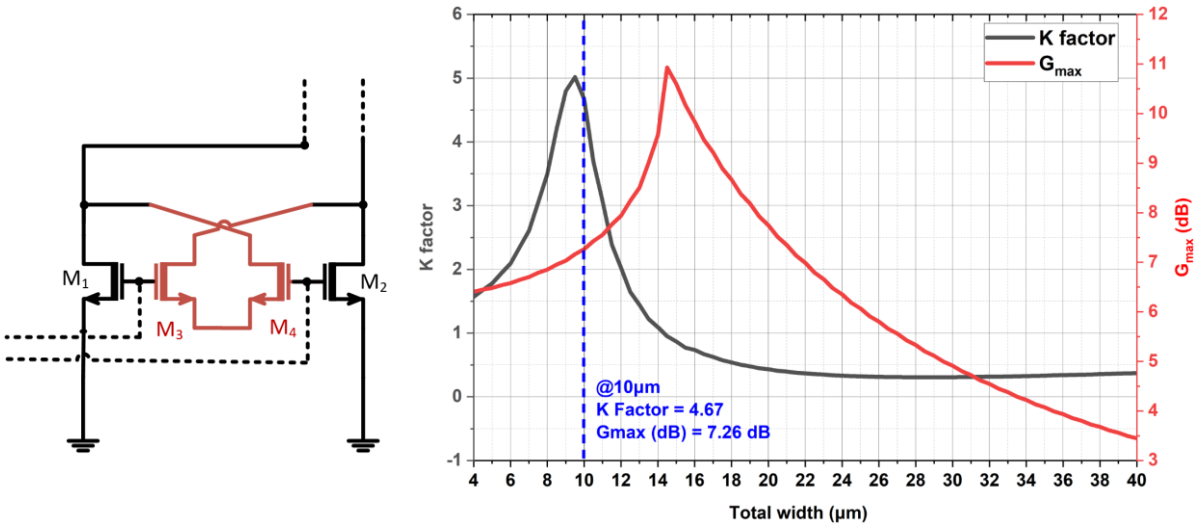


Figure 53. The common source buffer circuit with capacitive neutralization

The following methodology is adopted to design the buffer. First, the width of the transistors M_1 and M_2 need to be determined. This is achieved by dimensioning the g_m of 20 mS, which equals 50 Ω. The g_m will define the real part of the output impedance, whereas the transmission line TL_2 will act as a parallel stub to cancel the imaginary part of the output. The transmission line TL_1 acts as a high impedance point for the input signal to pass through the buffer transistor and not leak into the supply. C_1 acts here as the DC blocking capacitor, whereas C_2 is being utilized for matching purposes. The details are mentioned in the following paragraph.

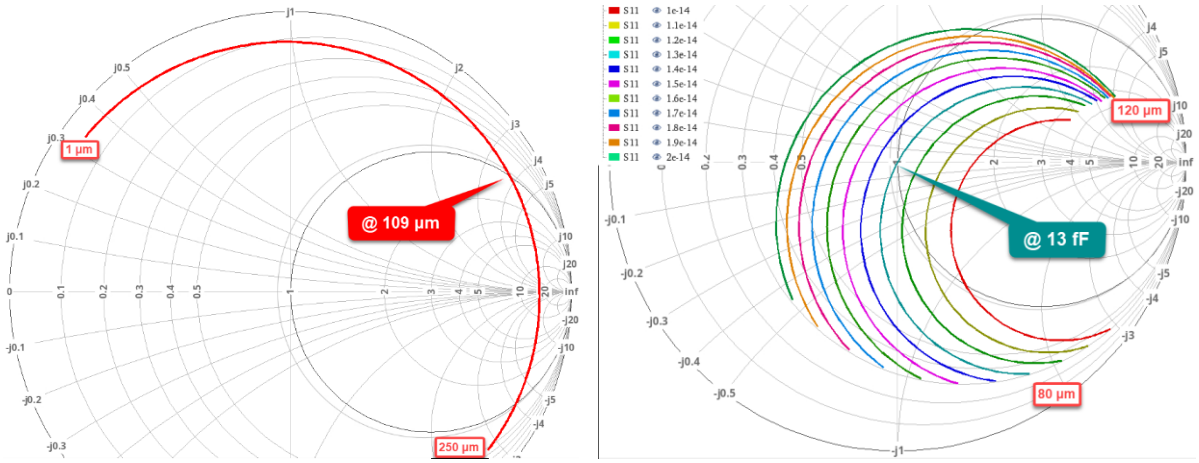
As discussed, first the core of the buffer is required to be determined, i.e., M_1, M_2, M_3, and M_4 are required to be determined first. The M_1 and M_2 are chosen to have a g_m of 20 mS. As a rule of thumb, the transistors M_3 and M_4 are dimensioned to be of the same width as M_1 and M_2 due to their equal parasitic capacitances. Thus, utilizing the M_3 and M_4 capacitances to enhance the stability of the core. This is demonstrated by the figure below, which depicts the plots of transistors M_3 and M_4 vs. K factor and G_{max} (maximum power gain). It is observed that 10 µm transistors are suitable to perform neutralization and to stabilize the buffer core with a K factor of 4.67 and a G_{max} value of 7.26 dB.



(a) Buffer Core (b) K factor and Gmax (dB) vs. total width

Figure 54. Buffer core schematic and simulation results

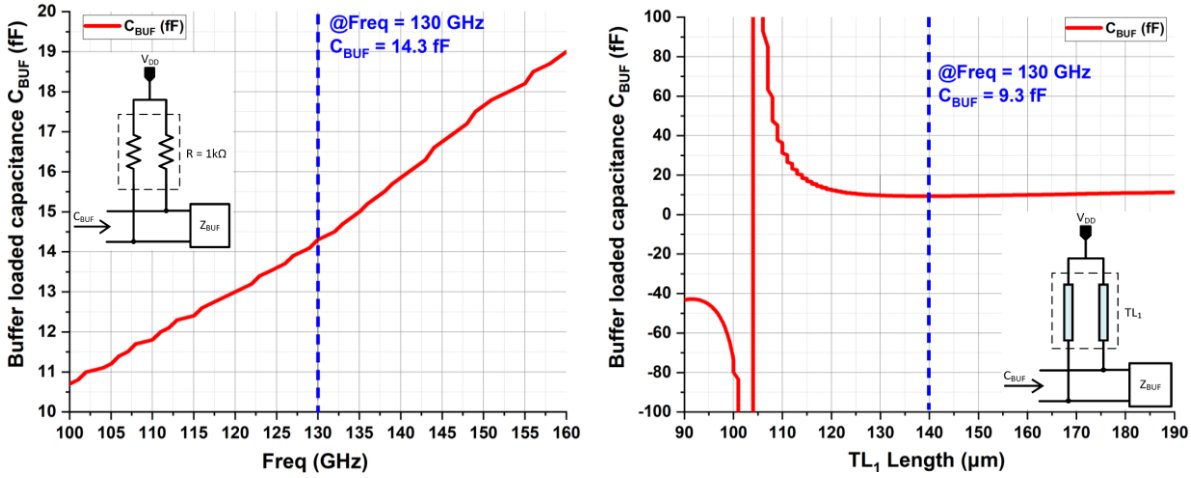
After the buffer core dimensioning, the next step is to perform impedance matching to 50 Ω at 130 GHz utilizing the transmission line TL_2 and capacitor C_2. The transmission line TL_2 length is swept over a range of 1 µm to 250 µm without capacitor C_2, and the length that takes the impedance close to the Smith chart "unity" circle is chosen, which is about 109 µm, as observed in Figure 55(a). After selecting the TL_2, the variable value of C_2 is swept over a fixed frequency of 130 GHz, and the value that intersects the circle of constant resistance of 50 Ω is obtained, as shown in Figure 55(b). Thus, the output is matched to 50 Ω. It is to be noted that TL_1 is not involved in the matching process, and its only purpose is to have a high impedance path for the signal not to pass through, and it reduces the buffer loaded capacitance towards the LC Tank. In these simulations, the TL_1 is replaced with a 1 kΩ resistance.



(a) TL_2 length swept from 1µm to 250µm (b) TL_2 swept from 80µm to 120µm at different C_2 values

Figure 55. TL2 and C2 values swept at 130 GHz

The loaded capacitance of the design is 15 fF with a resistor of 1 kΩ instead of a transmission line TL_1, which can be seen from Figure 56(a). This capacitive load of the buffer can be reduced by optimizing the length of the transmission line TL_1 until an optimum is reached instead of using a λ/4 transmission line for biasing. This is observed from Figure 56(b) where the loaded capacitance of the buffer is reduced by 34% with the reduction in the transmission line length (µm). The differential slow-wave transmission line is used for this purpose. Table 20 shows the final design parameters of this buffer design for the VCO.



(a) Loaded capacitance with R = 1kΩ (b) Loaded capacitance with TL_1

Figure 56. Optimization of the loaded capacitance of the buffer

Table 20. Design parameters of the common source buffer circuit

C_1 (fF)	C_2 (fF)	TL_1 (µm)	TL_2 (µm)
30	13	109	140

The performance of the VCO was verified after the buffer circuit. With a loaded capacitance of 9.3 fF, The oscillation frequency is reduced as compared to the previous designs and is currently oscillating at 124 GHz with a phase noise of -100 dBc/Hz at V_{TUNE} = 0V. With the loaded capacitance, the tuning range of the oscillator is also reduced and is at 3.74%. The

complete oscillator circuit is consuming 20 mW of power with a core inside consuming 9 mW, whereas the buffer circuit is consuming a power of 12.4 mW

Table 21. Performance parameters of the oscillator with common source buffer circuit design

Parameters	**V_{TUNE} (V)**	**Design Prototype 2**		
		A common source buffer circuit		
F'_{osc} - Simulated (GHz)	**0**	124.6		
Phase Noise (dBc/Hz) @ 10MHz	**0**	-100		
Output Power (dBm)	**0**	-1.5		
Signal Swing (Vp-p)	**0**	0.4		
Lower Freq (GHz)	**0**	124.6		
Upper Freq (GHz)	**0.8**	129.4		
FTR (%)	**0 to 0.8**	3.7		
Parameters	**V_{TUNE}**	**Oscillator circuit with biasing**	**Oscillator Core**	**Buffer Circuit**
V_{DD} (V)	**0**	1.2	0.6	0.8
I(mA)	**0**	16.4	15	15.5
P(mW)	**0**	20	9	12.3
FOM_T				**-172.5**

3.3.8 Comparison Buffer Design 1 and Buffer Design 2

The performances of the two buffer designs are almost identical, as illustrated in Table 19 and Table 21. The oscillation frequency of 124 GHz with a phase noise of -100. 3 dBc/Hz in source follower as compared to 124.6 GHz with -100 dBc/Hz in common source configuration design. The tuning range of both designs is identical. The overall power consumption is similar. The only improvement is observed in the output signal power of the oscillator designed with common source configuration with an output power of -1.47 dBm is higher as compared to -7.32 dBm in case of source follower. After a thorough analysis of all the parameters. The common source buffer design with capacitive neutralization is preferred due to two reasons:

- The design assists in ensuring the stability of the buffer circuit.
- The capacitive neutralization implemented in buffer neutralizes the gate to drain capacitances, thus assists in shielding the oscillator core with any changes at the output.

3.4 Layout Design

The complete circuit has been implemented on the 22nm fully-depleted silicon-on-insulator (FDSOI) process. The benefits of the FDSOI are low leakage, low power and reduction in parasitic capacitance to the substrate due to buried oxide layer. It also benefits from the back gate biasing in transistors [36]. The back gate allows the threshold voltage control by 84 mV/V, thus also known as body biasing [37]. The F_{max} of the nfet transistor is around 370 GHz, whereas the F_T is 347 GHz. For the pfet transistor, it is around 288 GHz of F_{max} and 242 GHz of F_T [38].

3.4.1 Layout Considerations

The 22nm process offers up to 10 layers metal stack, with eight thin layers (M_1 to M_8) and up to 2 ultra-thick metal layers (M_9 to M_{10}). The nominal supply voltage for this process is 0.8V. It was made sure that the design structure shall be as symmetric as possible. The traces carrying

current were made wide enough to offer a low resistive path for the current. The current per µm condition for the traces and vias were taken into consideration at every design phase. The voltage controlled oscillator is highly sensitive to parasitics, and any additional parasitics can dampen the oscillation of the tank. Therefore a lot of care was taken during the layout to reduce the parasitics where necessary. The layout was performed using the Cadence Virtuoso tool.

3.4.2 Floor plan

Figure 58 depicts the complete schematic diagram for the proposed voltage controlled oscillator and Figure 58 demonstrates the layout floor plan. It illustrates the relative sizes and area of the LC tank, CCP G_m stage transistors, PMOS current mirror, buffer circuitry and interconnects associated with all of these. The oscillator core is placed at the top and it includes the LC tank and CCP G_m stage. The PMOS current mirror is placed on top of it thus connecting to the supply voltage V_{DD}. Followed by the oscillator core, the buffer circuitry includes the buffer core transistors and the matching network. Two separate power supplies have been utilized. V_{DD} is 1.2V for the primary oscillator circuit including the oscillator core and the PMOS current mirror has a ground reference GND. $V_{DD,b}$ is 0.8V, which is for the buffer circuitry with a ground reference GND_b. The generated signal is extended towards the OUT+ and OUT- pads. GSGSG pads are being utilized for the RF out. The biasing and signalling pads are aligned on the four sides of the design.

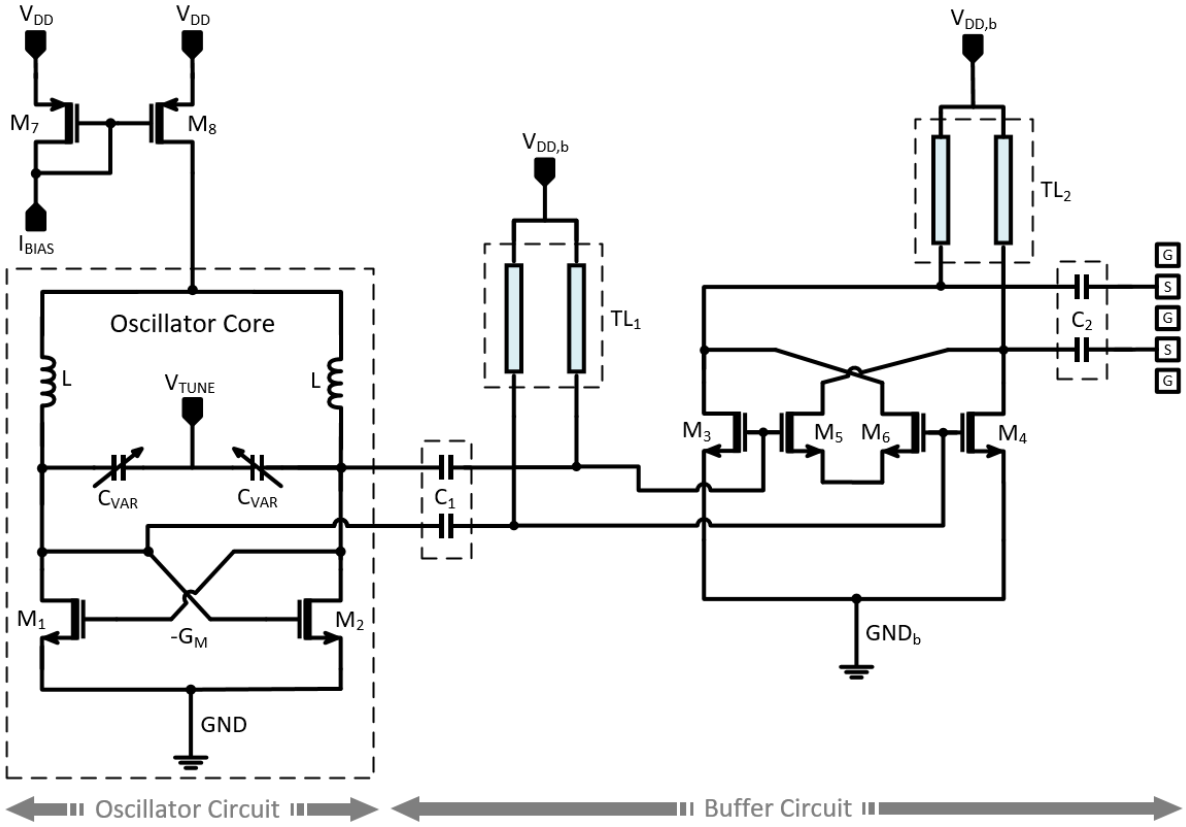


Figure 57. Proposed voltage controlled oscillator complete schematic diagram

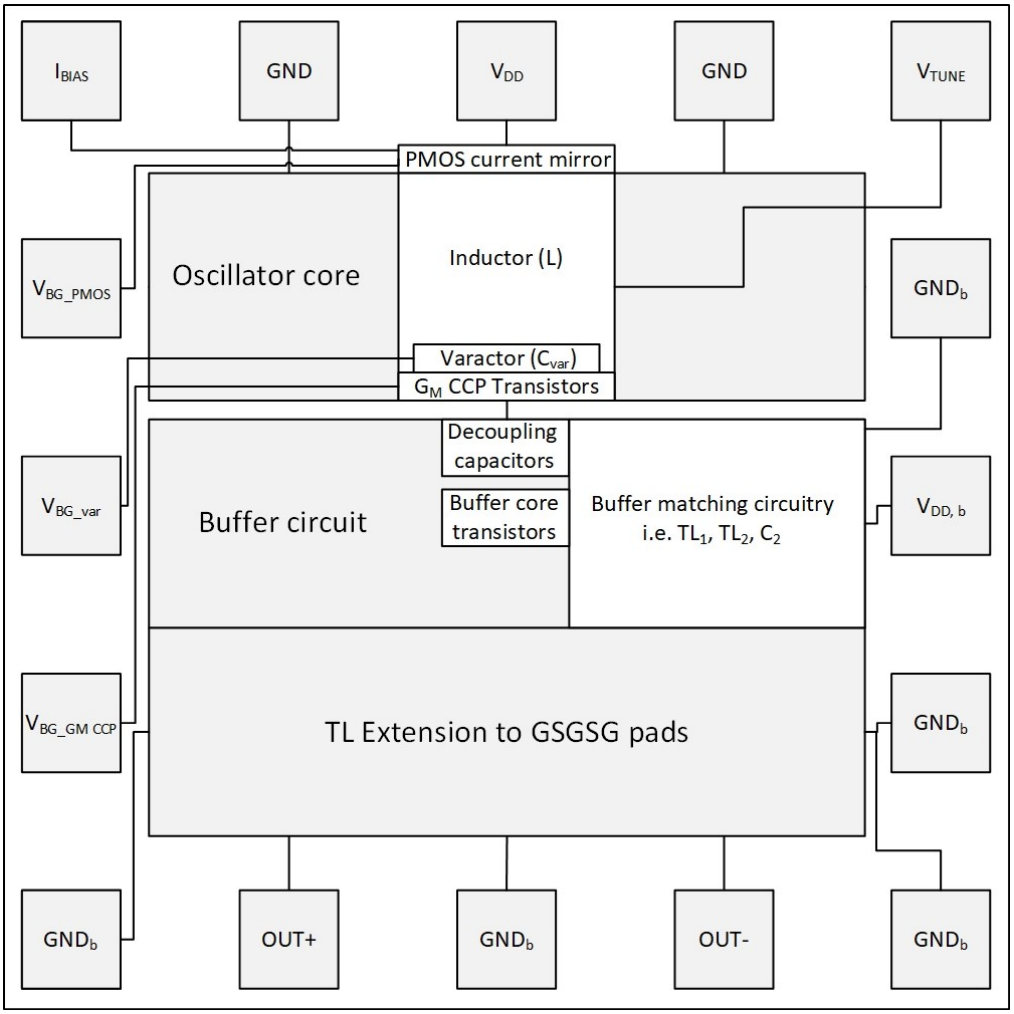
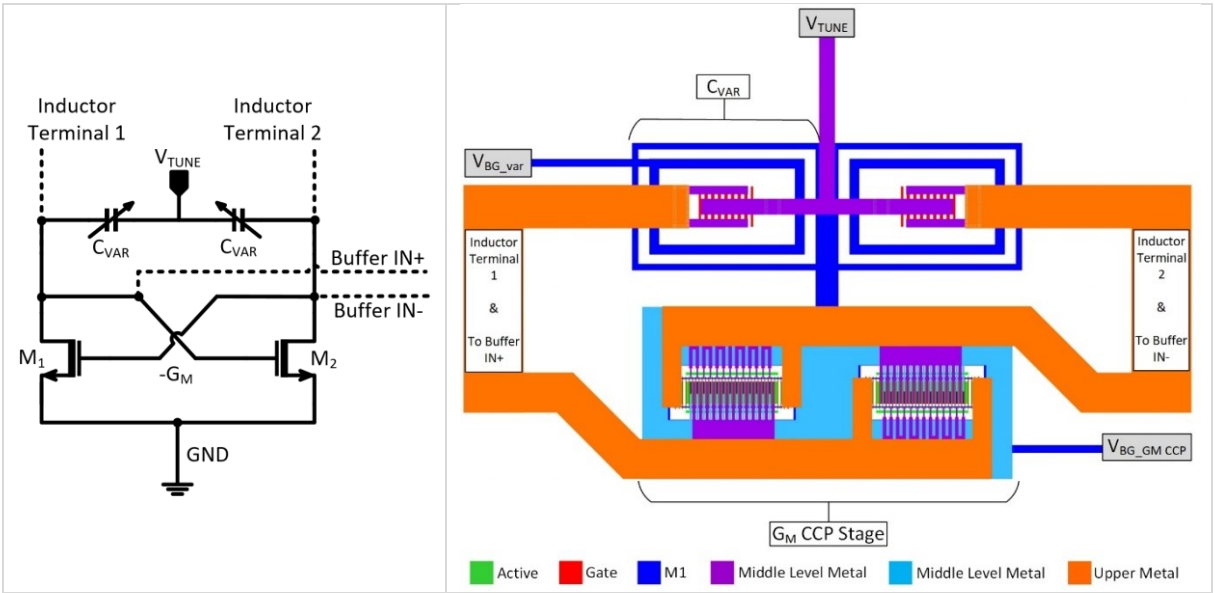


Figure 58. Floorplan of the proposed VCO design

3.4.3 Oscillator Circuit (Core + PMOS current mirror)

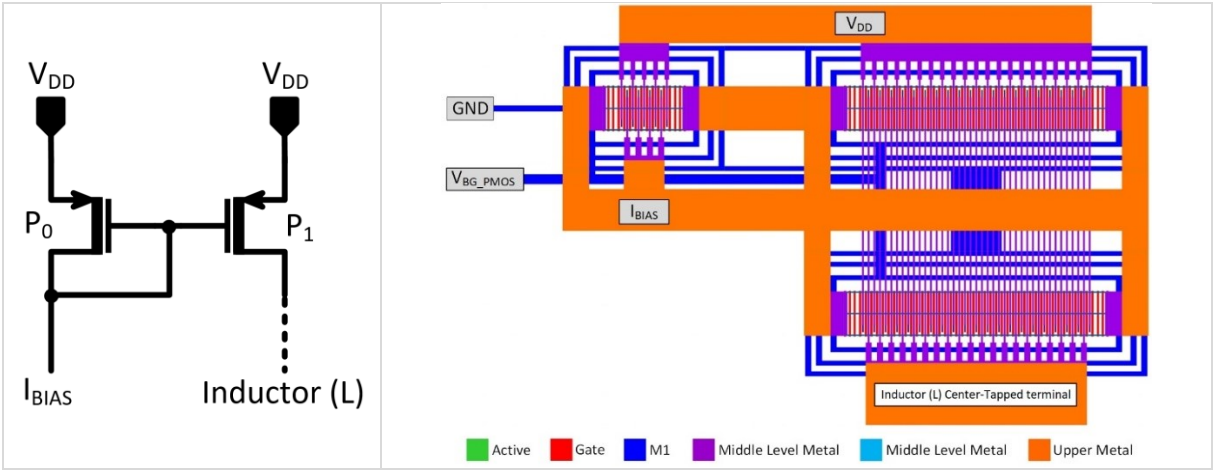
The layout of the oscillator core was designed first. Since the inductor (L) acquires most of the core area, the layout was designed to fit it with other RF components, which include the varactor and the G_m CCP stage. Figure 59 illustrates the varactor and the G_m CCP stage layout design. Since the G_m stage has its parasitics, the half strapped layout technique was adopted to reduce the parasitic capacitances C_{DS}, C_{GS}, and C_{GD}. Moreover, moving the drain and source connections away from the gate connection and to avoid less overlapping at different metallic layer assists in the reduction of parasitic capacitances. The gates are parallel fed with double gate contacts to reduce the gate resistance (R_G). The layout was lifted to the upper metal layer, which ran across the design and then connecting the gate of the varactor. The drain/source terminals of the varactor were lifted to the middle-level metal layer. It is then connected to the buffer input gate terminals and the symmetric inductor terminals. The parasitic extraction of the layout was performed.



(a) Schematic (b) Layout

Figure 59. G_m CCP pair and varactor layout design

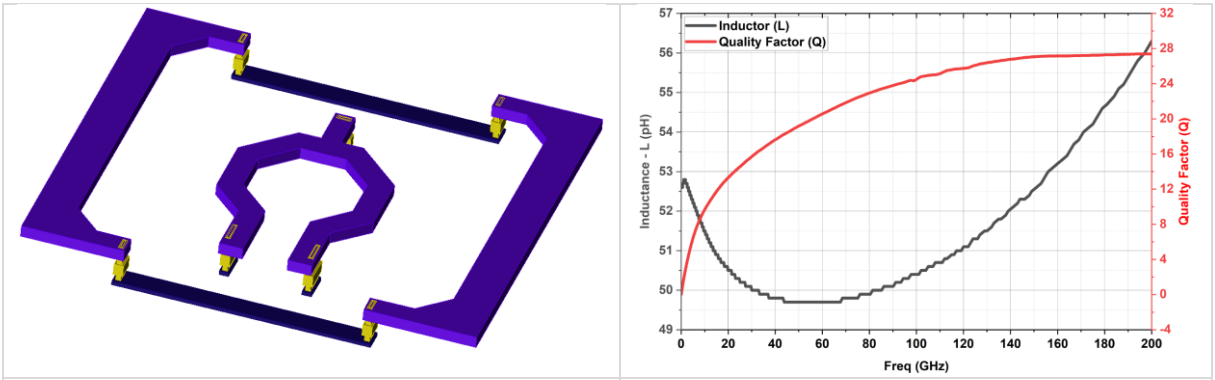
Figure 60 depicts the PMOS current mirror designed to have a 1:10 current division ratio. The drain/source terminals are lifted to the middle-level metal and then connected horizontally via stack to upper-level metal. These vertical and horizontal sharing connections between the gate terminals reduce the gate resistance (R_G) [39], also taking drain to the upper metal layer reduces the drain resistance (R_D), thus allowing more current to pass through. The parasitic capacitances are also reduced similarly, as described earlier in the designing of the G_m CCP pair stage.



(a) Schematic (b) Layout

Figure 60. PMOS current mirror layout

The symmetric single turn octagonal inductor is designed for differential excitation. The inductor is realized by utilizing the metallic layers M10, whereas as the ground planes were constructed by using the layer M10 and M8 as shown in the Figure 61(a). The inductor quality factor and inductance can be seen in Figure 61(b).

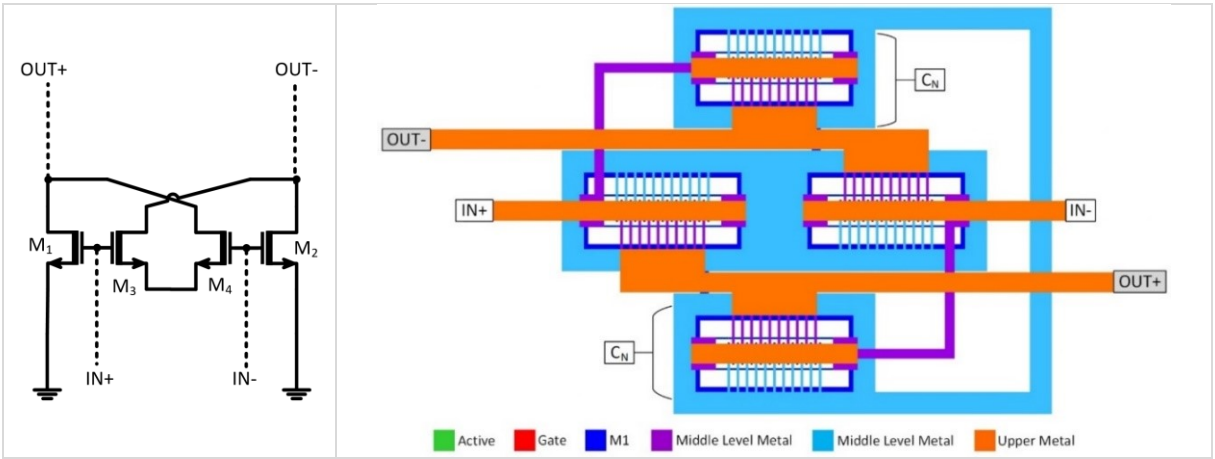


(a) Inductor layout design (b) Inductor performance

Figure 61. Inductor layout and performance

3.4.4 Buffer Circuit

The positive and negative output of the oscillator core is sent through the buffers and then through the transmission line extension until it reaches the GSGSG Pads. MOM (metal-oxide-metal) capacitor was utilized for the buffer output matching and decoupling of the buffer from the oscillator core. To reduce the terminal to substrate capacitance, only upper metallic layers were utilized for signalling. Figure 62 illustrates the buffer core design taken lifted up to the top metallic layers.

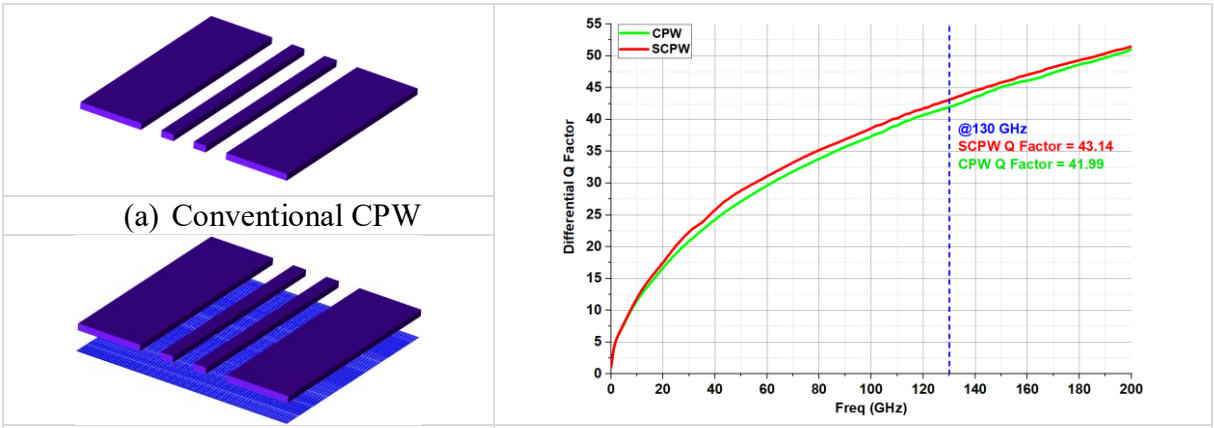


(a) Schematic (b) Layout

Figure 62. Buffer core layout with capacitive neutralization

3.4.5 Transmission lines

Slow-wave (S-CPW) transmission lines were utilized for the matching network of the buffer. The CPW transmission lines were selected for their better quality factor. For a fair comparison, the conventional and SCPW transmission lines were EM simulated with a constant line length of 100 µm, the signal to ground, and signal to signal width was kept constant at 10 µm. From Figure 63, it is clear that at 130 GHz, the slow-wave CPW provides a better quality factor as compared to the conventional CPW topology.



(a) Conventional CPW

(b) SCPW

(c) Differential Q Performance Comparison

Figure 63. Differential Quality factor comparison between conventional and SCPW transmission line

3.4.6 Final Layout Design

The top-level chip layout is being illustrated in Figure 64. All the individual component layouts discussed earlier have been combined in the oscillator and the buffer circuitry. The ground planes are constructed around it, connecting to the bias control pads and the output signalling pads for probing. The ground planes for GND and GND_b were constructed to create proper grounding loop around the circuity for the signalling lines to experience unified EM fields around it.

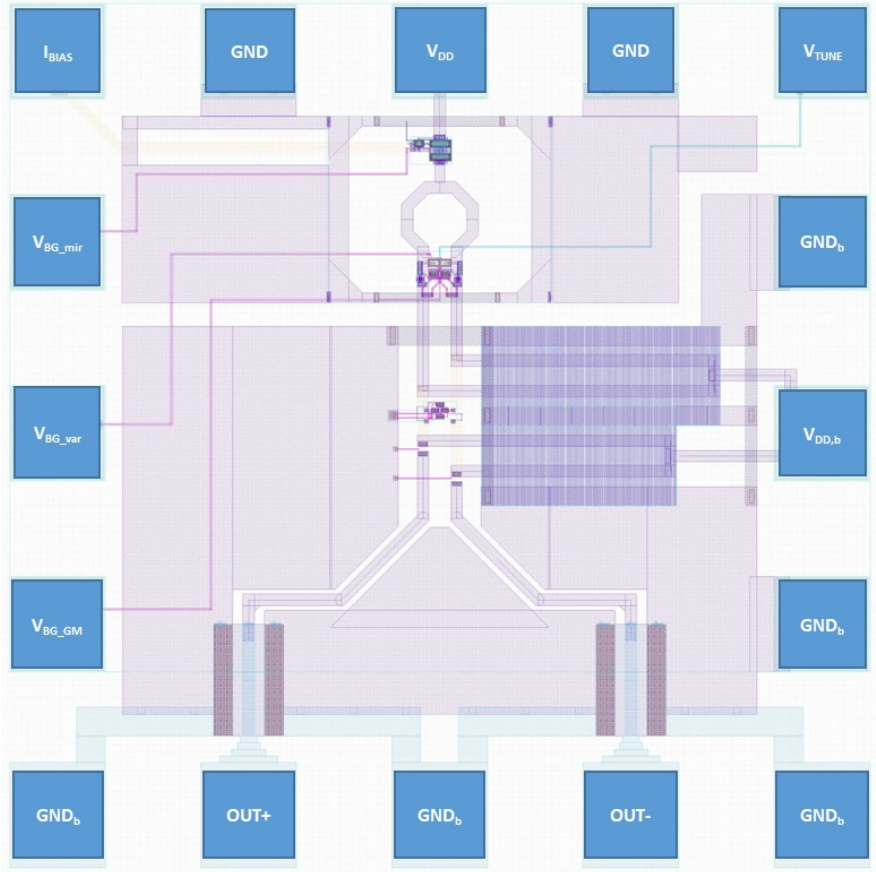


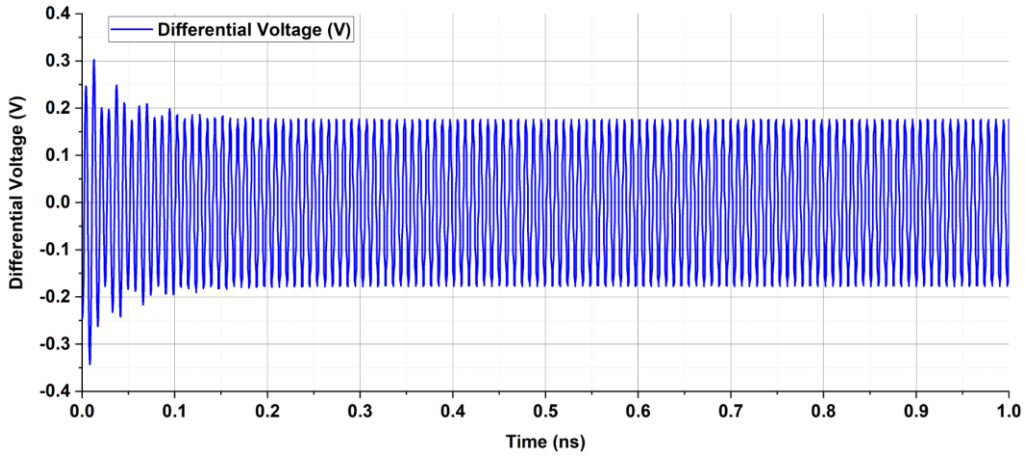
Figure 64. Final layout design of the proposed oscillator

4 PERFORMANCE EVALUATION AND SIMULATION RESULTS

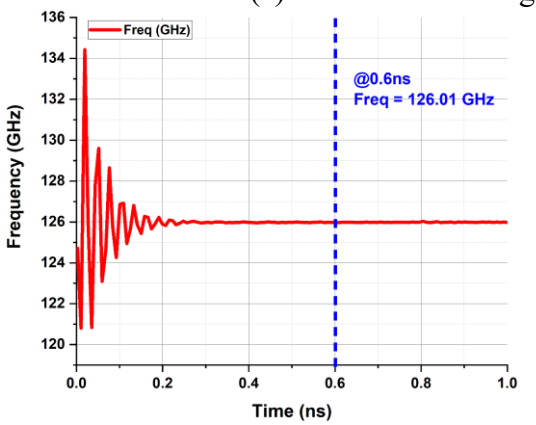
This section describes the post-layout simulation results and comparison with the state of the art VCOs in practice.

4.1 EM and Extracted View Co-simulations

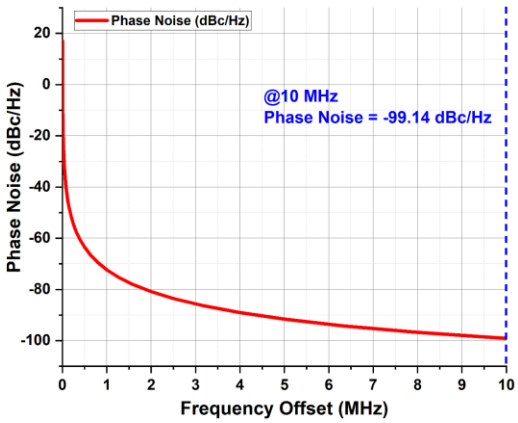
Parasitic extraction was performed for the oscillator core consisting of the G_m CCP stage and the varactor, and the buffer circuitry, including MOM capacitors and the buffer core. EM models were extracted for the structure, including the inductor, transmission lines, interconnects, ground planes, probe, and bias pads resulted in 19 and 21 port S parameter files for the oscillator and the buffer circuit. The performance of the design was analyzed and illustrated in Figure 65. The power supply for the oscillator and the buffer circuit is 1.2V and 0.8V. They dissipate power of 19.3 mW and 10.33 mW, respectively. The oscillator core consumes 8.98 mW. The outputs of the oscillator are terminated with 50 Ω load. PSS simulations have been performed to determine the waveform. The oscillator oscillates at a center frequency of 126 GHz with a phase noise of -99.14 dBc/Hz at 10 MHz offset frequency. Figure 65(e) shows the oscillator's frequency tuning curve in which the frequency ranges from 123.7 to 128.6 GHz, corresponding to a relative frequency tuning range (FTR) of 3.91%. The VCO has an output power of -1.87 dBm at a supply voltage of 1.2V. The output signal swing of the oscillator is 0.35 $V_{p\text{-}p}$ demonstrated in Figure 65 (f) and (g).



(a) Differential voltage taken from the GSGSG Pads

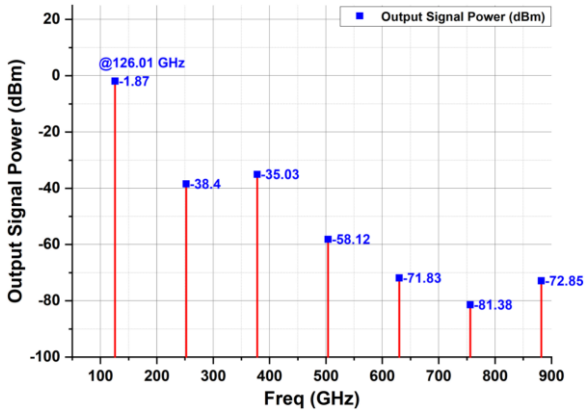


(b) Oscillation frequency (GHz)

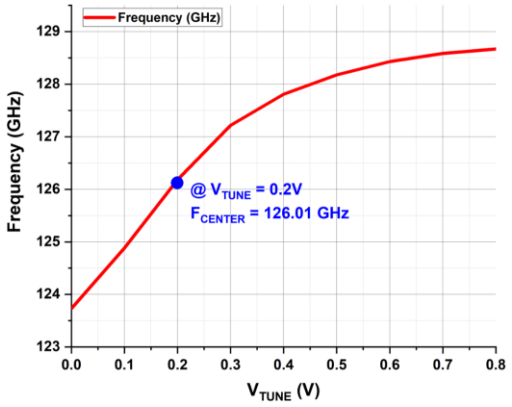


(c) Phase noise frequency offset (dBc/Hz)

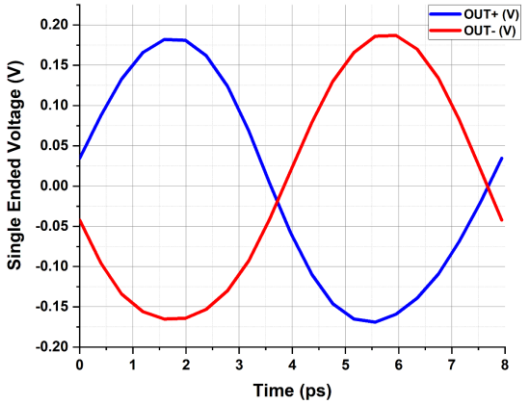
Figure 65. Differential voltage, frequency and phase noise of the proposed oscillator design



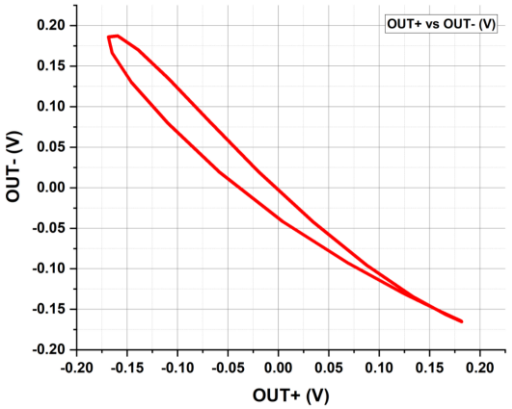
(d) Output power at different harmonics (dBm)



(e) Freqeuncy tuning range



(f) Single ended outputs



(g) Signal swing

Figure 66. Performance parameters of the proposed oscillator design

Table 22 illustrates the detailed parameters of the performance graphs discussed earlier. To observe the phase noise performance in Figure 65(c) at different offset frequencies, Table 23 demonstrates the phase noise performance at offset frequencies of 1 MHz and 10 MHz for different V_{TUNE} voltages. At the center frequency, the phase noise of -72.3 dBc/Hz at 1 MHz offset and -99.1 dBc/Hz at 10 MHz.

Table 22. Parametric Performance of the designed VCO

Parameters	**V_{TUNE} (V)**	**Proposed VCO Design Performance**
F'_{osc} - Simulated (GHz)	**@F_{center}**	126
Phase Noise (dBc/Hz) @ 10MHz	**@F_{center}**	-99.1
Output Power (dBm)	**@F_{center}**	-1.89
Signal Swing (Vp-p)	**@F_{center}**	0.35
Lower Freq (GHz)	**0**	123.7
Upper Freq (GHz)	**0.8**	128.6
FTR (%)	**0 to 0.8**	3.91

Parameters	**V_{TUNE} (V)**	**Oscillator circuit with biasing**	**Oscillator Core**	**Buffer Circuit**
Vdd (V)	**0**	1.2	0.6	0.8
I(mA)	**0**	16.4	14.9	12.9
P(mW)	**0**	19.68	8.98	10.3
FOM_T				**-172**

Table 23. Phase noise performance at different offset frequencies

Parameters	V_{TUNE} (V)								
	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8
F'_{osc} - Simulated (GHz)	123.7	124.9	126.0	127.2	127.8	128.2	128.4	128.6	128.7
Phase Noise (dbc/Hz) @ 1MHz	-74.2	-72.8	-72.3	-73.5	-75.2	-76.0	-76.6	-77.1	-77.4
Phase Noise (dbc/Hz) @ 10MHz	-100.2	-99.4	-99.1	-100.1	-101.3	-101.9	-102.3	-102.6	-102.7

4.2 Comparison with Published State-of-the-Art VCOs

This section presents the performance of the VCO compared to the previously published state of the art VCO. In Table 24, the performance of the designed VCO is summarized with high performance published VCOs in literature. For honest comparison below categories are distinguished: oscillators that employed the use of the CMOS process node and topologies that have performed better in D-Band frequency range. The well-known figure of merit discussed earlier in Section 2.3.4 is being used here to compare the performance of the VCO. It is observed that the proposed design performs relatively close to the VCOs designed implemented in the literature at frequencies around 120 GHz. Oscillating at center frequency of 126 GHz with a phase noise of -99.14 dBc/Hz, the oscillator achieves a FOM_T of -172, which is close to its competitors. All the presented oscillators have a comparable tuning range and power dissipation. The proposed design has a highest output signal power. It is to be noted that the FOM_T is highest for those published VCO designs that have achieved a relatively better phase noise performance at these frequencies even though the tuning range is low. The parameter that affects the designed VCO the most is the phase noise, which is currently -99.14 dBc/Hz, which comparable but not better as compared to the published designed VCOs.

Table 24. Performance comparisons of the State of the art VCO designs around 120 GHz

Reference	[40]	[8]	[41]	[11]	[9]		This work
Technology	130nm SiGe	90nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	22nm CMOS SOI
Topology	LC source degeneration and push-push	Cross coupled and push-push	LC type	varactor-less	LC type	LC type	LC type
F_{OSC} (GHz)	114	131	123	115	118.3	122.5	126
V_{DD}	1.2	1	1.2	0.7	1	0.8	1.2
P_{DC} (mW)	8.4	21	9.6	6.2	5.6	2	8.98
FTR (%)	2.1	1.7	1.3	4.4	4.4	7.8	3.91
Phase Noise (dBc/Hz)	-107.6	-108.4	-86.4	-99.1	-83.9	-83	-99.14
Phase Noise Offset (MHz)	10	10	2	10	1	1	10
Output Power (dBm)	>-22.5	>-28.6	-14	-2.5	>-28.5	>-28.5	-1.87
FOM_T	-179.5	-177.5	-172.4	-173.2	-175.7	-174.6	-172

The highest FOM_T is observed by the [39] utilizes push-push topology although suffering from a low tuning range and a decent power consumption of the core. The tuning range of the

fundamental port is 56.4-57.6 GHz and at the push-push port it is 112.8-115.2 GHz. Therefore, by adopting the frequency doubling solution and operating at half the desired output frequency ($f_0/2$) has benefitted this design to acquire a better phase noise performance. A similar example at 131 GHz of better phase noise is observed in [8] utilizing the similar push-push topology where the phase noise of -108.4 dBc/Hz is observed with a 10 MHz offset thus achieving a better FOM_T. The LC type implemented topologies published in the literature as seen in [40] and [9] at these frequencies have demonstrated the FOM_T to be slightly less compared to the ones utilizing the push-push topology which is mainly due to the phase noise performance. The phase noise and tuning range of LC type is mainly limited by the high quality inductors and varactors that determine the fundamental frequency of the VCO. The series resistance is a function of frequency and thus an increase in it degrades the Q factor thus in turn affecting the phase noise. Therefore, wide tuning range and low phase noise are contradictory demands while implementing the LC type topology. Another approach is to prevent the use of low Q varactor and to assist the VCO to reach higher frequency is being demonstrated in [11], where the varactors are not utilized in the design thus relying on the effective capacitance of the G_m CCP stage to form an LC tank. The supply is varied to achieve the desired tuning range. This approach has benefited the design to achieve a high frequency of 115 GHz. To conclude with the above mentioned comparison it can be concluded that the lower the input inferred phase noise, the better the VCO performance.

Another set of comparison is of the designed VCO is in the same process node i.e. 22nm CMOS SOI illustrated in Table 25. The VCOs have been implemented in literature at 60 GHz [5] and 80 GHz [6] with an FOM_T of -186 and -167 respectively. The currently designed VCO is oscillating at 126 GHz having an FOM_T of -172 which is at par in terms of the frequency of oscillation it has achieved in the same process since the FOM_T scales down with an increase in the frequency. The phase noise performance is also degraded with the increase in frequency with an estimated reduction of 3-4 dBc/Hz with every increase of 20 GHz in the oscillation frequency thus currently achieving a phase noise of -99.14 dBc/Hz.

Table 25. Performance comparison of state-of-the-art VCOs of the same process node

Reference	**[5]**	**[6]**	**This work**
Topology	LC type	LC type	LC type
F_{OSC} (GHz)	**60**	**80**	**126**
V_{DD}	0.7	0.6	1.20
P_{DC} (mW)	7.50	6.7	8.98
FTR (%)	34	1.8	3.91
Phase Noise (dBc/Hz)	-108.6	-104.7	-99.14
Phase Noise Offset (MHz)	10	10	10
Output Power (dBm)	-	-	-1.87
FOM_T	**-186**	**-167**	**-172**

To conclude, the LC cross-coupled VCO designed in this thesis is comparable to the state-of-the-art VCOs illustrated in Table 24 and Table 25. The designed VCO shows an excellent average FOM_T with a decent tuning range and phase noise respectively.

5 DISCUSSION AND FUTURE WORK

The study in this thesis has investigated the performance trade-offs and limitations in designing an on-chip voltage controlled oscillator. Although we succeeded in designing the LC tank VCO that is performing as desired, there are several areas of interest in future work related to work on this thesis. The most important one is to fabricate the designed chip to obtain a working VCO that verifies the simulation results. Apart from that, below are the considerations for future work to be performed to improve the design. The future work is divided into two categories. First, the modification in the design to improve noise performance. Second, the implementation of a different topology to reach higher performances in terms of frequencies.

As discussed earlier, the phase noise is an important characteristic of the design and shall be taken in account during the whole design process. The phase noise performance of the currently designed VCO is not very good compared to state-of-the-art VCOs. There is a limit to the phase noise level of a single VCO core due to the limited quality factor of the tank. Plenty of techniques can be implemented to improve the phase noise. A viable solution to lower the phase noise is to bilaterally couple several identical cores either resistively or inductively. Ideally, this can result in improvement in phase noise performance by 10.log(N) where N is the number of coupled cores as described in [42], [43] and [44] respectively. Apart from the phase noise, the circuits are prone to interference, thus resulting in common mode noise at the output. To mitigate this, a choke inductor is added in the buffer circuitry with one end connected to supply $V_{DD,\,b}$ and the other end connected to the common node of the circuit, an additional capacitor is added connecting from this node to the ground creating an LC resonance at an oscillation frequency thus rejecting the common-mode noise of the oscillator. This technique has been effectively implemented at 118 GHz fundamental VCO layout design [9] and in the LO buffer for mixer first receiver for the front-end of mm-wave massive MIMO arrays [45].

Another important consideration is the implementation of different topologies in practice. The below topologies are alternatives to the implementation performed in this design to achieve the 150 GHz target.

Varactorless: At a high frequency of operation, the Q factor of the varactor is worse than those compared to the inductors in the LC Tank. To realize an oscillator in the D band, the varactor size is getting smaller and smaller, thus having demerits of lower tuning range and Q factor. Therefore, the idea is to get rid of the varactor and utilize the parasitic capacitance C_{par} generated by the CCP G_m stage as part of the LC tank resonator. Since there is no varactor, the tuning is performed with the variation in the biasing voltage $V_{DD.}$ This technique has been successfully implemented in [46] and [11].

Push-Push topology: The maximum oscillation frequency that can be achieved by the fundamental oscillator design is primarily limited by the active devices utilized. The limitation for the maximum frequency of oscillation f_{max} is governed by the maximum available gain G_{max} of the transistor when reduced to unity. To extend the frequency range of the oscillator in a given technology, the harmonic content can be coupled out. Widely practiced at sub-THz frequencies, the technique utilizes the harmonics of the oscillators in yielding a better tuning range and phase noise performance implemented in [8], [40] and [22]. In general, the VCO is operated at a lower RF and this technique is utilized to increase it to the required mm-wave frequency without introducing additional noise. Therefore to achieve a sweet spot in terms of the quality factor of the LC tank, it is worth realizing the VCO at lower frequencies and then utilize the push-push configuration to obtain the required mm-wave frequency.

6 CONCLUSION

The primary objective of the thesis work was to study, design and simulated a voltage controlled oscillator for FMCW radar applications operating in D-Band targeting to 150 GHz. In the beginning, a literature review on key fundamentals aiming at a good understanding of each step of the design flow was done. The state-of-the-art VCO practices were reviewed to define good strategies in the design process. The methodology to implement the proposed design was being discussed in detail. The extensive background research was conducted in the selection of VCO topology, inductors, varactors, transistors and trade-offs associated to it in order to achieve the desired oscillation frequency, tuning range, noise performance and power consumption. A brief study was conducted on the tank Q factor which is dominated by the low Q factor of the varactor. A balance was created to choose a smaller varactor compromising on the frequency tuning range and a high value inductor to improve the tank Q factor thus assisting in the phase noise. The G_m cross-coupled pair stage parasitic capacitance contributed in dragging down the oscillation frequency and reduced the frequency tuning range. The performance limitation of the design was analyzed. A comparative study of the two buffer designs i.e. source follower and common source was conducted. The buffer loaded capacitance was reduced by optimizing the transmission line during the interstage matching.

Overall the simulated performance of the final designed VCO is comparable to the state-of-the-art published VCOs with certain demerits. First, the high phase noise is due to the low Q factor of LC tank. Second, the fixed capacitance of the G_m cross-couple pair stage and the buffer contributed in the reduction in the frequency tuning range. With all these drawbacks, the proposed LC VCO design oscillates at 126 GHz with a tuning range of 3.9%. It achieves FOM_T (Figure-of-merit) of -172 dBc/Hz, and phase noise of -99.14 dBc/Hz at 10 MHz offset, core power consumption is 8.9 mW from a 1.2 V supply in a 22nm SOI CMOS process. The frequency of oscillation lies in the D-Band and is suitable for FMCW radar applications. To reach the 150 GHz mark, future work and improvement will be taken into consideration.

7 REFERENCES

[1] J. C. Scheytt *et al.*, "Towards mm-wave System-On-Chip with integrated antennas for low-cost 122 and 245 GHz radar sensors," in *2013 IEEE 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, SiRF 2013 - RWW 2013*, 2013.

[2] B. P. Ginsburg, S. M. Ramaswamy, V. Rentala, E. Seok, S. Sankaran, and B. Haroun, "A 160 GHz pulsed radar transceiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, 2014.

[3] H. J. Ng, J. Wessel, D. Genschow, R. Wang, Y. Sun, and D. Kissinger, "Miniaturized 122 GHz system-on-chip radar sensor with on-chip antennas utilizing a novel antenna design approach," in *IEEE MTT-S International Microwave Symposium Digest*, 2016.

[4] A. Visweswaran *et al.*, "9.4 A 145GHz FMCW-Radar Transceiver in 28nm CMOS," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2019.

[5] C. Zhang and M. Otto, "A wide range 60 GHz VCO using back-gate controlled varactor in 22 nm FDSOI technology," in *2017 IEEE SOI-3D-Subthreshold Microelectronics Unified Conference, S3S 2017*, 2018.

[6] T. Lim *et al.*, "Slow-wave coplanar strip line based Low-power 80-GHz voltage control oscillator on 22-nm FDSOI technology," in *Asia-Pacific Microwave Conference Proceedings, APMC*, 2017.

[7] P. C. Huang, M. Da Tsai, H. Wang, C. H. Chen, and C. S. Chang, "A 114GHZ VCO in 0.13µm CMOS technology," in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2005.

[8] P. C. Huang *et al.*, "A 131 GHz push-push VCO in 90-nm CMOS technology," in *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*, 2005.

[9] W. Volkaerts, M. Steyaert, and P. Reynaert, "118GHz fundamental VCO with 7.8% tuning range in 65nm CMOS," in *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*, 2011.

[10] Y. Zhao, B. Heinemann, and U. R. Pfeiffer, "Fundamental mode colpitts VCOs at 115 and 165-GHz," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2011.

[11] W. Badalawa, S. Lim, and M. Fujishima, "115GHz CMOS VCO with 4.4% tuning range," in *European Microwave Week 2009, EuMW 2009: Science, Progress and Quality at Radiofrequencies, Conference Proceedings - 4th European Microwave Integrated Circuits Conference, EuMIC 2009*, 2009.

[12] D. B. Leeson, "A Simple Model of Feedback Oscillator Noise Spectrum," *Proc. IEEE*, 1966.

[13] U. Yodprasit, R. Fujimoto, M. Motoyoshi, K. Takano, and M. Fujishima, "D-band 3.6-dB-insertion-loss ASK modulator with 19.5-dB isolation in 65-nm CMOS technology," in *Asia-Pacific Microwave Conference Proceedings, APMC*, 2010.

[14] T. Kosugi, A. Hirata, T. Nagatsuma, and Y. Kado, "MM-wave long-range wireless systems," *IEEE Microw. Mag.*, 2009.

[15] W. Tan, T. Wu, Z. Xing, Y. Peng, H. Liu, and K. Kang, "A 21.95-24.25 GHz Class-C VCO for 24 GHz FMCW Radar Applications," in *2019 IEEE MTT-S International Wireless Symposium, IWS 2019 - Proceedings*, 2019.

[16] *Analog Design Essentials*. 2006.

[17] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw Hill Higher Education, 2003.

[18] J. O. Plouchart, H. Ainspan, M. Soyuer, and A. Ruehli, "Fully-monolithic SiGe differential voltage-controlled oscillator for 5 GHz wireless applications," in *Digest of*

papers - IEEE Radio Frequency Integrated Circuits Symposium, 2000.
[19] J. Kim *et al.*, "A Power-Optimized Widely-Tunable 5-GHz Monolithic VCO in a Digital SOI CMOS Technology on High Resistivity Substrate," in *Proceedings of the International Symposium on Low Power Electronics and Design*, 2003.
[20] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE J. Solid-State Circuits*, 2000.
[21] F. Lenk, M. Schott, J. Hilsenbeck, and W. Heinrich, "A new design approach for low phase-noise reflection-type MMIC oscillators," *IEEE Trans. Microw. Theory Tech.*, 2004.
[22] C. Cao, E. Seok, and K. K. O, "192 GHz push-push VCO in 0.13μm14; CMOS," *Electron. Lett.*, 2006.
[23] M. Da Tsai, Y. H. Cho, and H. Wang, "A 5-GHz low phase noise differential colpitts CMOS VCO," *IEEE Microw. Wirel. Components Lett.*, 2005.
[24] J. A. Hou and Y. H. Wang, "A 7.9 GHz low-power PMOS colpitts VCO using the gate inductive feedback," *IEEE Microw. Wirel. Components Lett.*, 2010.
[25] K. Ma, *Low-Power Wireless Communication Circuits and Systems: 60 GHz and Beyond*. Pan Stanford Publishing, 2018.
[26] C. Sandner, F. P. Pavan, A. Gerosa, and A. Neviani, "Transformer-Based Dual-Mode Voltage-Controlled Oscillators," *IEEE Trans. Circuits Syst. II Express Briefs*, 2007.
[27] Z. Safarian and H. Hashemi, "Wideband multi-mode CMOS VCO design using coupled inductors," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2009.
[28] X. Liu, Z. Huang, J. Yin, and H. C. Luong, "Magnetic-Tuning Millimeter-Wave CMOS Oscillators (Invited Paper)," in *Proceedings of the Custom Integrated Circuits Conference*, 2019.
[29] N. Yanay and E. Socher, "Wide tuning-range mm-wave voltage-controlled oscillator employing an artificial magnetic transmission line," *IEEE Trans. Microw. Theory Tech.*, 2015.
[30] *Low Power VCO Design in CMOS*. 2006.
[31] Ekta Sharma, "Design of millimeter wave VCO based on slow-wave transmission lines." *Micro and nanotechnologies/ Microelectronics. Université Grenoble Alpes, 2016.*
[32] M. Danesh, J. R. Long, R. A. Hadaway, and D. L. Harame, "Q-factor enhancement technique for MMIC inductors," in *IEEE Radio Frequency Integrated Circuits Symposium, RFIC, Digest of Technical Papers*, 1998.
[33] E. Sharma *et al.*, "Design of a 77-GHz LC-VCO with a slow-wave coplanar stripline-based inductor," *IEEE Trans. Circuits Syst. I Regul. Pap.*, 2020.
[34] N. Deferm and P. Reynaert, "Differential and common mode stability analysis of differential mm-wave CMOS amplifiers with capacitive neutralization," *Analog Integr. Circuits Signal Process.*, 2014.
[35] L. Li, P. Reynaert, and M. Steyaert, "A low power mm-wave oscillator using power matching techniques," in *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*, 2009.
[36] S. N. Ong *et al.*, "22nm FD-SOI Technology with Back-biasing Capability Offers Excellent Performance for Enabling Efficient, Ultra-low Power Analog and RF/Millimeter-Wave Designs," in *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*, 2019.
[37] S. S. Rao, B. Prautsch, A. Shrivastava, and T. Reich, "Body biasing for analog design: Practical experiences in 22 nm FD-SOI," in *Proceedings - 2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuit and Systems, DDECS 2017*, 2017.

[38] S. N. Ong *et al.*, “A 22nm FDSOI technology optimized for RF/mmWave applications,” in *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*, 2018.

[39] C. Zhang, F. Zhang, S. Syed, M. Otto, and A. Bellaouar, “A Low Noise Figure 28GHz LNA in 22nm FDSOI Technology,” in *Digest of Papers - IEEE Radio Frequency Integrated Circuits Symposium*, 2019.

[40] P. C. Huang, M. Da Tsai, G. D. Vendelin, H. Wang, C. H. Chen, and C. S. Chang, “A low-power 114-GHz push-push CMOS VCO using LC source degeneration,” *IEEE J. Solid-State Circuits*, 2007.

[41] C. Cao and K. O. Kenneth, “A 140-GHz fundamental mode voltage-controlled oscillator in 90-nm CMOS technology,” *IEEE Microw. Wirel. Components Lett.*, 2006.

[42] L. Iotti, A. Mazzanti, and F. Svelto, “Insights into Phase-Noise Scaling in Switch-Coupled Multi-Core LC VCOs for E-Band Adaptive Modulation Links,” *IEEE J. Solid-State Circuits*, 2017.

[43] S. A. R. Ahmadi-Mehr, M. Tohidian, and R. B. Staszewski, “Analysis and Design of a Multi-Core Oscillator for Ultra-Low Phase Noise,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, 2016.

[44] F. Padovan, F. Quadrelli, M. Bassi, M. Tiebout, and A. Bevilacqua, “A quad-core 15GHz BiCMOS VCO with -124dBc/Hz phase noise at 1MHz offset, -189dBc/Hz FOM, and robust to multimode concurrent oscillations,” in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2018.

[45] L. Lotti, G. LaCaille, and A. M. Niknejad, “A 12mW 70-to-100GHz mixer-first receiver front-end for mm-wave massive-MIMO arrays in 28nm CMOS,” in *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2018.

[46] Y. S. J. Shiao, G. W. Huang, C. W. Chuang, H. H. Hsieh, C. P. Jou, and F. L. Hsueh, “A 100-GHz varactorless CMOS VCO using source degeneration,” in *IEEE MTT-S International Microwave Symposium Digest*, 2012.